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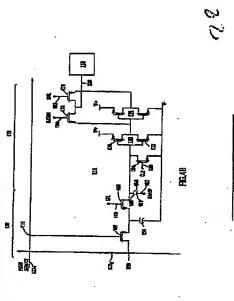
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Analog pixel drive circuit for a display device

An analog drive circuit (114) that drives a plast electrode (118) in response to an analog esmole derived from a victor exprai. The analog other circuit comprises a sumple selection section (128) and a drive ing a sumple load period. The drive signal generator generates a drive signal and applies the drive signal to the plast electrode during a display period that fallows. signal generator (128). The cample selection section receives and temporarily stores the analog sample dur-

the sample load period. The drive signal is composed of a sequence of a first temporal portion and a second corporal portion. The first temporal portion has a time temporarily stored in the sample selection section. The second temporal portion is the temporal complement of the first temporal porifon



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### Desoription

# Field of the travention

[0001] The hveration relates video and graphics deplay devices, to suralog dradis for othing the picture demanticipales) or video and graphics deplay devices, and, in particular, to analog dradis for driving the picpliar elements of a display device based on an eladropagical material.

# Background of the Invention

(1002) A substantial need exists for various types of video and graphico dizzleg debress with introored positionaries or for example, a need exists for ministure video and graphics dizzleg debress that are small crough to be integrated into a halmst or a pair of dizzless so that fary can be uran by the uses. Such wearable dizzleg devices would replace or supplement as the conventional dizzleg devices and dise devices. In particular, weatable dizzleg devices and dise devices in particular, general dizzleg devices and dise portation computers, possible privary, audostratisty devices and provide grazies in brightness, better receits it in a larger battery file than conventional order metric or outde-examilitation ord displays, disease and an advice or of the displays devices are in the procorate advicementary, in wide or second of contrained applications of wearable dizzleg devices and in virtual resulty systems.

pures and in vintual ready systems.

10009 Minthurbord displays based on cafinderay thas or conventional parts of system displays have not been accessful in meeting the demands of wearched displays have not been accessful in meeting the demands of wearched displays far flow weight and emal date. Of greater promise is a mixer display and earth of the type described in this displays of all the controlled into this displays of all the described in this displays and which is incarporated into this displays includes a redisplay of which is not display includes a redisplay of making the bight northalism their uses a knowledged orystal (PLI) material as its light control element.

This strated from management of thems of themselvents.

proof) The spatial light modificator of the PLC-beased intro districtly used described is driven by a dispital drive districtly used described is driven by a dispital drive districtly one promotivation and only dispital driven districtly one organic computer, the graphics card of a personal computer, the energy video styral into a digital bistream cultable for driving the special light modition. The converter converts the analog video signal into a time domain bronzy weighted digital drive of the form of the modits. For The Bronz duritions of the bits of the fine domain than y weighted so that de the least significant bits, where or list the curration of the mortice guilding and the least-significant bits, where n is the numbor of bits represented by 8 bits, the duridion of each in restrictly and certain most-digital in represented by 8 bits, the duridion of each most-digital or each issued of each in rest-digital world wideo signal in represented by 8 bits, the duridion of each most-digital control most-digital in expressment by 8 bits, the duridion of each most-digital control most-digital in each signal.

tear bit. Driving the pixels digitally means that the pixel driver must be capable of dranging state several times of the reallog victor signal. The existing speed must be storier from the duration of the existing speed must be storier from the duration of the existing speed must be storier than the driver constitution in each study be capable of high-speed operation, which increazes the power demand and capacites of the micro-display system. On the other head, the lang time duration the most experience that do the display of the display drive signal is existent the migran of the first period.

the least-eignificant bits for of the clighel of the aigness all the pixels of the special light modulator, followed by the referred to above typically locate the converter referred to shove external of the micro display and connect the converter to the micro display by a high-speed digital link. The convertor time multiplexes the digital drive sigrats for transmission though the digital fink as follows: ned-least-eignificent bite of the digital drive signals for all the pixels, and so on frough the most-significant bits of the digital drive signals for all the pixels. The digital serting each frame of the component wideo signal (10005) Practical embodiments of the micro display within the frame period of the component video signed. The digital first, its driver and receiver must be capable of switching at a switching appeal shorter than the durafon of the least-significant bit, yet remain static for times corresponding to the durations of the most-elgrificant bits. ink must be expecte of transmitting all the bits repre-20

pood) in addition, the conventer requires a large, highspeed buffer memory to convert the parallel, realer-ecan order folgels eignals persented from the enelogy video eignal to a thironare agnal for each color component. This increase the cost and power requirements of the conventer.

locating the digital serial link can be eliminated by locating the converter in the micro digitaly lead, but reducing the converter in the micro digitaly lead comparably of the micro digitals. Microwat, ministurbing the converter for fit is in micro digitals, increases the cost of the converter. Finally, reducing the converter does not reduce its curval cost and complicity. (1000g) What is needed is a ministure digitally derive moderals in response to a video signal or graph its data and fast does not suiter from the size, weight, completally and cost descharateges of the convertions digitally-other micro display.

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full-size video and graphics display that would provide effective attemative to conventional carticolaray tubos and fiquid crystal displays. ۶

# Summary of the Invention

ple keal period. The drive eigensi generator generates a drive signal and applies the drive signal to the pixel elec-trode dufing a display period that follows the sample for driving a point electrodic in response to an analog chould comprises a sumple selection scotlan and a chive stored generator. The sample calection codion receives and temporarity stores the analog cample curing a sam-The drive signal is composed of a The invention provides an analog dive circuit poral porfor. The first temporal porton has a time dura-tion substantially proportional to the analog sample lemporarily stored in the sample selection section. The second temporal portion is the temporal complement of sample derived from a video signal. The amplog drive sequence of a first temperal portion and a second temthe first temporal portion. lond period.

The sample authout gate opens either during or prior to the display perfed and is disposed between the sample The santule storage section may include a sample output gate. The cample selection gate opens campio otorage element, a campla salection gate, and a ple to the compte storage element and is closed during during the sample load period to actril the analog sama display period that follows the sample load period. stange element and the chive signal gonerator. (10012) The drive signal generator may include a com-

is corrected. The ramp eignel has a duration equal to is connected, and a second input to which a ramp signal perator that generates the drive signal and that comprises a first input to which the cample selection section The comparator may have a detection sense set by a serse compol signal having opposite states in the display period. (2013)

consecutive frames of the video signal. In this caso, the enable drive circuit additionally includes first and secswitching arrangements. The first switching in consecutive display periods. The second exitating anargement alternately connects the sample aprage section to (a) the second input and (b) the first input of (0014) The ramp signed may have a non-linear slope Brangement alternately connects a ramp signal to (a) the fest input and (b) the second input of the comparator the comparator in consecutive display periods. g

\$

include an inverter that generates the othe signal, a The offive signal generator may efternatively capacitor and a switch. The capacitor has a first electrade connected to the Irput of the inventor and to the comple selection section, and a second electrode connected to a rump algnal having a curation equal to the Appley period. The switch discharges the capacitor to provide gamma correction. prior to the depley poriod.

8

ewitch is coupled to a reference signal that has a stable oqual to a prodetermined inverter threshold voltage The othe signal generator may additionally include a coupling capacitor and an additional switch The coupling capacitor couples the input of the inverter to the sample selection section. The additional switch lamporarily connects the output of the inverter to the input of the invertor prior to the display period. The when the additional switch connects the output of the reverser to the input.

The showe-martitioned sequence of the tiral be a first sequence of the first temporal portion and the second temporal portion and may have a duration equal to one half of the display period, and the drive signal generator may generate the othes signal in a first electrical state cluing the first temporal portion and in a sectemponsi portion, in which the other signal is in the first electrical state. The first temporal portion and the secand temporal portion may be in any order in the second amparal partion and the second temporal portion may and electrical state during the second temporal portion. in this case, the dilive signal generator may generale the of a second sequence of the first temporal portion, in which the drive signal is in the second electrical state, and the second enquence. The second sequence rectores the DC baldrive signal additionally composed ance of the pixel. 8

a pulse heaving a second potarity, apposite the linet polarity, at the beginning of the second portion. To generate this drive signal, the drive signal generator may include When the analog drive circuit is for driving an electro-capical material having a bicable disractoritie, polarly at the beginning of the first tamporal portion and the drive signal may be composed of pulse having a first En E.C.-coupled output. 8 R

Brief Description of the Drawings

### 900

Figure 1 shows the structure of a display device that incorporates the analog drive circuit according to

Figures SA-SD illustrate how analog samples are derived from the wideo signal and distributed to the make drive clout of each phal in the phal array of the operial light modulator shown in Figures 2A-2D. the tree fames of the video signal shown in Fig-ures 3A-3C stored in the sample adoction section of the analog drive circuit of an exemplary pixel of Figures 2A-2D strow details of the spadal light mod-Hours SE shows the analog samples derived from ulator of the display device shown in Figure 1.

8

Figure 9F shows the drive signals generated by the pics shown in Figure 3.E. Rgure 4.A is a block diagram showing the pixal gnating drive directli in response to the amelog som-

device that incorporates a first enfortiment of the out of a first embodiment of a monodrome display Figure 48 is a coherratio diagram of the livel array and the sample derivation and distribution ciranalog of the circuit according to the invention.

Figures SA-SD are waveform degrams illustrating he invention.

enthodiment of the enalog offive circuit according to

ivation and distribution circuit shown in Figure 4A Figures 7A-7G are waveform diagrams illustrating he operation of the embodiment of the analog drive the uperation of the embodiment of the display Figures 64-6R are waveform diagrams Bustneting the operation of the embodiment of the sample derdavice shown in Figure 4A.

that inhitinizes variations in the effective offset of Figure 8 is a cohemetic diagram of a variation on the first embodiment of the analog othe circuit according to the invention that incorporates circuitry chould shown in Figure 48.

Figures 6A-60 are waveform degrams Bustrating the operation of the offset minimizing circuity of the the drive signal generator.

Figure 10A is a block diagram showing the pixel auit of a second embodiment of a monodiname display device that incorporates a coord enfocument of the analog drive circuit according to the Invenentey and the sample derivation and distribution cirembodiment shown in Figure 8.

Figure 108 is a schematic diagram of the second embodiment of the enalog drive circuit according to the Invention

ing the operation of the entodiments of the display doeloo, the sample derivation and distribution drauit and the smalog other drauit shown in Figures 10A Figures 11A-11O are waveform diagrams Buchtul-

Figure 12 is a block daggam of an exemple of a switched-sense comparator suitched for use in the embodinaris of the analog dave draid shown in Figures 108, 15C and 16B.

a variation of the second embodiment of the mone-Houre 18 is a block diagram showing the pixel array and the sample derivation and distribution circuit of Figures 14A-14F are waveform diagrams Bustrating the operation of the embodiment of the sample drame display device.

Jerheiton and distribution circuit shown in Figure

.

Figure 15A is a block diagram showing the pixel array and the panellel-load sample derivation and distribution circuit of a first embodiment of a color display device that incorporates a third embodiment of the enalog drive circuit according to the invenFigure 158 is a schomatic daynam of the third embodiment of the analog drive chauft executing to

Figure 15C is a schematic diagram of a fourth embodiment of the enable drive circuit according to Houre 16 is a block diagram showing the pixel array embodiment of the analog drive circuit according to and the sarial-load sample derivation and distribution circuit of a second embodiment of a color disthe invention for displaying a color video signal. the invention for displaying a color video signal. device that incorporates the the invention. À

Detailed Desoription of the Invention

2

device 10 according to the invention first includes the reflective spetial light modulator 100. Other principal components of the display device are the light cource 15, the polarizer 17, the beam splitter 19, the analyzer Figure 1 shows the structure of the display 21 and the eyepieco 28.

2

driver 67 that drives the LEDs 69-71. The LEDs are of other fight-emitting devices whose output can be repidly modulated may alternatively be used as the light source (0021) The light source 15 is compassed of the LED different colors and are independently driven in a color ance to Figures 15A and 16. Fower or more LEDs, or display device, as will be described below with refer-15. As a further alternative, a white light source and a ight modulator may be used. The light modulator mod-8 ĸ Ŗ

ukace the amplitude of the light autout by the light saures and, in a cate design device, autilitionally modulates and, in a cate of the light output.

policy | The light source 15 generates light that possess through the policy rate 15 generates light that possess through the policy rate 17. The been spiriter 19 relicads a zation of the reflected fight is either undumped or is rotated through 90°. The reflected fight passes to the the tayer 31 of electro-optical material (the electro-opti-cal kayer), to be described below, the direction of polarinaction of the polarized light from the polarizer towards the spetial fight enodulator 100. The reflective electrode 85 located on the surface of the substrate 89 of the spetial light madulator reflects a teasion of the brokeni potentized fight. Depending on the electric field across ucar's eye E through the beam splitter 19, the analyzer 3

(DUZ3) The eyepiece 23 focuses the light reflected by the reflective electrods 85 at the user's eye E. The eye plece is shown as a single convex lars in Figure 1. A more complex aptical enengement may be used to form a low-abenation image of the decired apparent size at 21 and the eyepiece 23. the user's eye.

The direction of polarization of the analyzer 21 is aligned parallel to the direction of polarization of the polarizer 17 so that light whose direction of polarization has not been rotated by the apatial light modulator will pess through the analyzer to the user's eye E, and light trough 90° by the epatial light modulator will not pass frough the analyzer. Thus, the analyzer prevents light direction of polarization has 8

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whose directors of potentration has been retained by the against light menkatine from resoluting the users eye. Consequently, the quates light mediatine appeared light of dark to the users depending on the applied electrical of the dark to the user depending on the applied electrical of the dark to the user depending on the applied electrical. When the speaks light modulator appears dark it will be said to be into ONF state. The direction of potentialized of the analyzer can elemanishly be amarged orthogonal to that of the poderizor. In this case, the speaks light modulator operates in this expected some best light modulator operates in this expected some best light modulator operates in this expected for the speaks to pleave to be described by illuminating the speaks of potential light modulator during the basiness portical to be described between

(0008) The optical annugament shown in Figure 1 may also form the basis of a full-time video or graphics display. The inventors have demonstrated such a full-size order of the control of the such a full-size of 450 mm. This display device was made by increasing the intensity of the light source 16 and by inspirating the eyesteep 23 with intensitying optica that form an image of the reflective electrodes 50 on a suitable or man image of the reflective electrodes sequentially fluminated by this of the first printsy octors, or portificient primary octor, can be used in a full-size octor.

reparation to degrees 22 with moughlying agains that for man finge of the reflective electrode 55 on a suis-burder of the coron. A single spatial forth moutator sequencially Eurificated by Reith of the fore primary colons, or parallel ferminated by Reith of effects for the contract of the size of contract of the contract of the size of the size of the contract of the colon of the contract of the colon of the contract of the contract of the colon of the service of the colon of the colon of the service of the colon of the

opposed on the surrect of the transparent cover St. The oldcatches 5's is focused on the surrace of the servi-contralor substants 99.

FOCCT An electro-optical majoral is a material hawing on optical property that depends on an applied electric field. For example, in the optical premy ennous shown in fight. For example, in the optical premy ennous shown in light impliciting on the effection of polarization of light impliciting on the electro-optical layer depends on the direction of an electric field applied in the layer. In other electro-optical materials, notation of the direction of polarization may depend on the strength of the decicion of polarization may depend on the strength of the decicion of polarization may depend on the strength of the decicion of polarization may depend on the security of other electro-optical materials amy depend on the electric field applied to the leyer.

(100.2) Some electro-optical materials have a bistrible characteristic in such materials, the optical property of the metalistic is est by upplying a chort-duration electrical puts. The material will heap the optical property set by the decircular busine until the material is reset by applying a forth duration optical puts in the optical drescine. Betale electro-optical materials have the advantage that the electrical putson that other can be three-only to trisinously one an odditional businos provid to be described busine, need rust be provided. This provides a flarger businous efficiency companied with elec-

(0029) In the preferred embodiment, the electro-optical material. The direction of the electric field system between the transferred electric field system between the transferred electrode 83 and the reflective observed to determines whether the direction of sight implying on the ferce decir makeful sandwiched between the electrodes is trasted or not. In other embodiments, a conventional nematic liquid carsis are sundoments, a conventional nematic liquid carsis are simply of the electro-optical material. In this case, the single of the electro-optical material, in this case, the single of the electro-optical material. In this case, the single of the electro-optical material is not optication in midside or not.

[8030] To enable the depily derive 10 to display an image instead of mentaly completing the pessage of light is the tomes of light is come 16 to the custor of light is the described size divided into the characterial and of pixel electrodes is divided into the characterial and of pixel electrodes, enablight, an enablo divide discuss of which are shown at 118, in addition, an enablo divide discussed in the size and which are shown at 118, in an enablo divide discussed in the size and these fines describe and the portions of the doctro-quitted layer 31 and the common electrode on the doctro-quitted layer 31 and the common electrode as oversigning the pixel electrode and the portions of the doctro-quitted layer 31 and the common electrode as examples one of which is set stored.

se shown at 112.

(DOST) When the decato-optical layer 31 is composed of a femodectric method, the direction of the decator tool applied between each pixal decatod, such as the pixal decatod, such as the determine whether the decation of polarisation of the layt reflected by the pixal decatord is rotated through 60° or not, and thus whether the corresponding pixal, such as the pixal into a pixal substantial frought 60° or not, and thus whether the corresponding pixal, such as the pixal into the pixal appearation of the loss. When the pixal appears think the beautiful to the beautiful to the pixal appears that it to be into OFF estable.

(2002) The optical desacteristics of the pixels of the species of the species light modulator 100 are binary, light from the light source 15 and reflected by the pixel either pesses frough the analyzer 21 to the usar's eye E or does not the user's eye. The light is modulated by choosing a pess through the enetyzer to the user's eya. To produce a grey scale, the apparant brightness of each pixal is besic time period that will be called the illumination varied by temporally modulating the light that reaches perhod of the spattal light modulator. The spatfal light modulator is illuminated through the Kumination period and each plosal is set to its ON state for a first temporal portion of the Illumination perfort, and to its OFF state for a second temporal portion. The second femporal portion constitutes the remainder of the Blumination period, and is thus complamentary to the first temporal portion. Altomethydy, the OFF state may precede the ON state. The traction of the liumination period constiluted by the first temporal portion, during which the pixel is in its ON state, deformines the apparent brightness of

To maximize the service the of the spetial light

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modulator, the DC balance of each pixel must be main-

9 2 8 e to zoro. This is accomplished in practice by driving the timolintatival of the electric field conventional (non-bisseate) femolectric material during the first temporal portion is rarely equal and opposite to that applied during the second temporal porifor, additional measures must be taken to restore the DC behance of the pixel. The DC belance of the pixel is roctored by driving the pixel so that the electric field applied to the famoelectric material of the pixel everages ing the illumination period is followed by a second sequence of the first temporal portion and the second temporal portion, the second sequence constituting a Authors perforf, in the first and second lemporal por-forts of the balance portod, the eable of the drive signal is the same as first during the second and first samporal portions, respectively, of the Bumination perfort. To prepixel electrode so first the first sequence of the first tempotal purtion and the spoord temporal portion constitutvert the balance period belowing each Rumination period from causing the display device 10 to display a uniform, grey image, the light generated by the light course 15 to modulated so that the spatial light modula-for 100 is only illuminated cluring each illumination period and to not illuminated cluring the following batŝ

The Munication period and the balance period light modulater. The display period of a monodrame display may correspond to the frame period or the piccollectively constitute the claptay period of the spatial ture period of the video signal, for example.

As noted above, the drive signal required to drive a histable electro-collect material during the litumiquently, no balance period need be provided, and the character of the flurnington period can be extended from netion period can be inherently DC balanced. Conseabout 50% of the display time to about 100% of the dis-5

The principles just desorbed may be extended to onsible the spatial Eght modulator to generate a color light source 15 Pluminates the spattal light modulator with light of a different color cluming the flumination period of each display period. Each pixel is ent to its ON state for a fraction of each of the three flumination periods, and to its OFF state for the remainder of the liturity outs, and to its OFF state for the remainder of the liturity. by the color components of a color video signal, and three display periods are defined for each frame of the color video signel, one for each color component. The for example. Making the dioplay period the same image. In this case, the spatial light modulator is driven each of the three deformines the apparent enturation and has of the pixel. to one-third of the frame period of the color video Burnington periods in which the pixel is in its ON state The display periods of a color display may each correnation period. The fraction of good

The epatial light modulator 100 will now be

lator is composed of the electro-optical layer 31 sandwidhed between the transparent cover 37 and the semiconductor substate 39. The transparent cover, twent common electrode 33, which may be a layer of inclum the code (ITO), for example, is located on the 20. Referring first to Figures 2A and 28, the light moduwhich may be a tith glass plate, for example, is exparated from the substrate by the spacers 108. The transheide surace of the transparent cores, facing the subdescribed in more detail with reference to Figures 2A

of the substate 39. The exemplary pixel is shown at 112. The drawings froughout this disclosure show pixel would be composed of, for example,  $640 \times 480, 800 \times 600$  pixels,  $1280 \times 1024$  pixels,  $2044 \times 1125$  pixels, or An array 102 of pizets is located on the surface anays with only four ploats in each dimension to simplify the drawings. In a practical embodiment, the pixel erray some other acceptable two-dimensional arrangement of 800

For each pixel in the pixel array 102, an arratog ventional comicanductor processing on and under the surface of the substrate 39. The analog drive cloud of the eigenplay pixel 112 is shown at 114. The analog which external observation connections are made by additional layers of conductors (not shown). The surface of fine shartests, and the above-mentioned layers of conductors, are covered by the incutaling layer 116. The reflective pixel electrode 118 of the pixel 112 is focated othe circuit is composed of transistors, capacitors and other aircuit elements (not shown) interconnected by one or more layers of conductors (not shown). The anatog drive charits of the potets constituting the pixel array log offive circuit. The pixal effectode is connected to the drive circuit according to the invention is formed by con-102 effe connected to one another and to pads filrough on the surtace of the insulating layer overlaying the ansoutput of the enselog drive circuit 114 by the conductor 120 which pesses through an aperture formed in the (850E) 'n

(0040) In the pixel 112, the areatog drive circuit 114 genericates a drive signal that is explice to the pixel electrode 118. The drive signal applied to the electrode has a 1 state and a 0 state. The 1 state may be a high volve. the electro-quical layer 31 overlaying the posel elao-trade rotates the direction of potentialing alight falling age state, and the 0 state may be a low voltage state, for example. The state of the drive signal applied to the pixel blactrode determines whather or not the portion of auth sats the apparent brightness of the pixel by applying on the pluet as described above. The analog drive cirthe drive signal to the pixel electrode in response to an snatog sample derived from a video signal. During each above-described Illumination period the drive signal starts in one state, corresponding to the ON state of the pixel, for example, and remains there for the first temporal portion. Before the end of the illumination period, the this signs switches to the other state and remains Insufating layer.

dhe droil sets the apparent exturation and hus of the pixel by applying dhe stones that hun the pixel ON for tractions of three consecutive flurination periods that second temporal parties. The fraction of untration period for which the pixel is in its ON When the video eignst its a color video signet, the analog depend on the firms color components of the color determines the apparent brightness of the pixel

ventrari analog video signal is enovn. However, this is not critical, the video signal may be composed at digital The video signal may be a conventional analog graphics data such as is led to a computer graphics adaption or is generated by a digital video or television data to an enaing wideo signed, or to derive directly from rideo signal such as la generated by a conventional computer graphics exteptor card, victeo or tedevision or. In the exemples to be described belon, a conreceiver. In this case, conventional additional chaultry ind shown) is provided to convert the digital graphics the digital graphics data the analog samples that are distributed to the arralog drive circuits of the ploats.

100421 Figure 2A shows the pixels enterged in the two-dimensional pixel enray 102 on the suskees of the substrate 8S. The sample derivation and distribution circuit recolved via the video input 106 to the pixel array and generates. The various firming sand, control eigenis required by the pixel array. Signals are distributed from els by busses, representative once of which are shown schomatically at 181 and 193. 104 is also farmed in the substrate 39. This circuit distitutes analog samples derived from the video signal the sample derivation and distribution circuit to the pix-

ples are distributed to the pixel constituting the pixel array 102 by the sample distribution chould 124. Each spall receives at least one sample of each frame of the video signal. The boorforn in the frame of the video signal. The boorforn in the frame of the video signal where the sample is derived comaganist to the location of the pixel in the pixel array, as thesitated in Figure 2C is schematic representation of the electrical enrangement of the special light modulator 100. The arrelog campling circuit 122 receives a video signal wa the wideo input 106 and dorives a stream of analog samples from the video signal. The analog sam-Harres 34-30. FOOds

(1044) Figures 3A-8C respectively show examples of three consocutive frames of the video signal received emay 102. Each line is shown divided into four eegcorresponding to the four pixels in each row of ments 123, 123, and 123, i.e., the second segment of the cocond line of each frame, see indicated by the horcircuit in response to each segment of For example, the analog samples derived from the sagvia the video input 106. Each framo is shown divided Into four lines comesponding to the four rows of the plast the pixel array. The arrating sample generated by the the video signal is indicated by a short horizontal line. zontal lines 125, 125, and 125, respectively.

receives the enalog sumples 125, 125, and 125, respectively derived from the segments 128, 128, and 128, of the frames. These segments extend from 14-The row and column numbers of the pixels in wit 124 distributes the analog comples are indicated in second pixel in the second row of the pixel array, and so the pixel amay 102 to which the sample distribution cir-Figure 30. For example, the exemplary place 112 is the aray atong to 1/2-way atong the second line of each frame of the video signal.

derived from the wideo signal via the sample input and temporarity stores the sample until the sample is an rectaid by the cirve signal generator 12th Eigure 3E actions the samples derived from the three frames of the video signal shown in Figures 24-3C stored in the sample selection ection of the pixel 112. doctrical arrangement of the pixel 112 in the two-dimensional pixel array 1102. The remaining books have the same electrical arrangement. The pixel is composed of the suriog drive circuit 114, the cuptur of which is connected to the electrode 118 by the conductor 120. The analog drive obtail is composed of the sample selection accion 125, and the drive signal generator 128. The sample selection section has a sample input Figure 20 is a schemetto representation of the (Hours 2C). During each frame of the video signal, the 127 connected to the sample distribution clicuit 124 sample selection section receives an analog sample (3004G) 22 ₽

eraiog sample stared in the sample calculon section 125 during the picture poriod of the previous frame and, eignel generator generatos the drive signal with a period corresponding to the above-described despity portiod. Figure 28 Forws an example of the drive signal gener-ated by the anakog drive drout 114 h mapones to the aretag samples shown in Figure 3E. Each of the display aretag samples shown in Figure 3E. Each of the display periods of the drive signal is composed of an illumina-tion period and a beliance period of equal durations. The proportional to the vollege level of the corresponding analog sample. This can be seen by comparing the durations of the first temporal portions I TP of librariain response to the sample, generates a chive eighal and applies the chive signal to the electrode 118. The chive drive signal generator additionally generates the drive signal in the 1 state for a first temporal portion 1 TP that conditutes a fraction of each flumination period that is fon periods shown in Figure 3F with the corresponding voltage fevrets shown in Figure 8E. 8

state. Firstly, the other signes changes to the 1 state for the account. Namporal portion 2. The constituting the remainder of the balance period. The duration of the stituting the remainder of the illumination period, and (10043) The drive signal is generated so that it remains also for the first temporal portion 1TP of the balance period. The first temporal portion of the balance period in the O state for the second temporal portion 2 TP con-8

EP 0 983 960 A1 purifon of the drive signal is different in each of the fires illumination periods, depending on the voltage ferol of the respective cample. In each tollowing belence period, the drive signal is in the 1 state for the second temporal portion, and is therefore in the 1 state by a firme that is complementary to the charation of the 1 2

(0049) In the example shown in Figure 25; the display period of coold frame begins immediately after the end of the display period of the previous frame. In some below with reference to Figures 4A and 48, the drive embodiments, such as the embodiment to be described waveform is generated intomittently, and a period in

withon the drive signal is generated in a neutral state is birdeposed between consecutive display periods. It (1969) The waveforms just described are those required to drive a electro-optical material that leads a bistate described. With be exporent to a person of ordinary skill in the art that circuits, such as bitable electropolical material by capacitatively or a.c. coupling the outsat of the atroat to the pixel electrode. [USS1] Rights 4A end 4B show as first practical ambiodiment of the decuity of the spatial light mechanic frose to be described below, for generating such waveexample, an analog drive circuit capable of generating the waveforms just described can be adapted to drive a forms can easily be adapted to generate the waveforms required to drive a bisrable electro-optical material. For 100 in more detail. In particular, Figure 4A shows in more detail the sample derivation and distribution drout and distributes the samples to the individual pixels. Roue 48 shows the analog drive circuit of one of the pixels 104 that derives artalog samples from the video signal in detail and will be described below. In this embadiment, sample selection circuits that perform the rou-wice distribution function of the sample distribution chcircuits of the pixels. The analog campling circuit 122 of the pixel array 102, and the sample section direct in cuil 124 shown in Figure 2C reside in the analog othe generales a stream of analog samples for each column each pixel performs the row-wise eelection from the sample stream in (2500)

highly-simplified 4 x 4 amay of places to simplify the to a morrochrome display dovice based on a drawing and the explanation. A variation that provides a This embodiment will be described with refercolor display device will be described below with raterence to Figure 15A and 15B.

ACTRO SIGNAL Y viz the victeo imput 106. As will be analog othe count additionally has a roup input and The analog sampling circuit 122 receives the described in more detail below, the analog office drout of each pixel in the pixel array 102 has a semple input additional inputs for various fining and control signals (not shown in Figure 4A). Each analog drive drouit and a row selecting out. For example, the pixel 112 has the cample input 150 and the new select input 110. The delivers a chive signal to the electrode first overlays it.

log camples received by each column of pixels are derived depends on the location of the column in the pixel singly, as described above. An analog cample of amity are connected to a column bus fret is in turn connected to a respective output of the analog sampling chount 192. For example, the sample imputs of the phase In the second column, where the exemplary pixel 112 is located are connected to the column bus 131,2. The location in each line of the video signs! wheree the aneevery line of the video signal is ted to the sample liqual of each smaleg drive circuit.

stato in the flumination period.

(2064) The row select inputs of all the pixels in each row of the pixel early 102 are connocted to a row soloral but that is driven by a corresponding output of the row video signal, the row selector sats the row select bus 1384, connected to the first row of pixels to the 1 state, selector 134. For example, the row select inputs of the plikele in the second row, where the exemplary pixel 112 is located, are connected to the row select bus 183<sub>2</sub>. An at its sample trout only when its row select input is the 1 stats for exemple. The row selector sequentially sets: Adeo signal. During the first line of each frame of the first column. The column bus of each octum leads the arelog camples to all the pixels in the octumn, but the analog camples are only eccepted by the pixels in the enabg drive circuit can accept a analog sample present The row select busses to the 1 state at the line rate of the and sels the remaining row select busses to the Distata. The sampling circuit 182 sequentially feeds analog camples of the first line of the video signal to the column busses in order, starting with the columntus 181, of the ×

nected to the first row of placts to the 0 state, and sats the row select bus 188<sub>2</sub> connected to the second row of equentially feeds enalog samples of the second line of (10055) At the end of the first line of the video signal, row selector 134 sets the row select bus 133, conducts to the 1 state. When the sampling circuit 132 the video signel to the column busses, the analog samof pixels. This process is repeated with the row salector sequentially setting the remaining row select busses 1883, and 1884, to the 1 state until each pixel in (0056) The part of the analog sempling circuit 122 that ples are only accepted by the pixels in the second row the pixel erray 102 has accorded a different analog sample derived from the frame of the video signal. 34

defives analog samples from the video signal and the sample estation obtain 124 that feeds the analog sample input of the analog drive circuit of each of the playes in the play array 102 will now be The video signal is fed from the video input 106 to the buffer amplitter 196. In addition to buffering the video signal, the buffer ampiliar may actificonally 500

drange the dynamic range and DC level of the video agent to meet the dynamic range and DC level require ments of the analog office chruits of the light modulato

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100. The video signal 's, output by the busiler ampilier is led to the campilier may alter to the busiler ampilier may alternatively be comitted.

The busiler ampilier may alternatively be comitted.

loossy. The sampling drault 122 is composed of one carries earth-diskly drout for each column of the public array 102. To camprily the deming, the SM drauls of the Other 139, tran 139, tran by the fine the SM drauls 139, and 139, tran bear oritified. Each of the SM drauls has a signal input S, a control from Column Series input S, a control from Column Series input S, and 139, trans bear the Column Series input S, and 139, trans bear oritified in received the video signal Y<sub>C</sub> cultur by the buffer arrayider 139. The control from Column Series 139, The control from column Series 139, is connected to the column or the Column Series. The sample the output of the Solumn or prosts. For example the output of the Stocker. The camprile the output of the SM circuit 139, is connected to the column but 131, connected to sample impute of the mallog drive circuit of 180 protein in the first column.

um.

(10039) The column selector 140 receives the chock signed and the PMEL from the clock generator 142. The chock signed and the horizontal spire often expected cock signed and the horizontal spire optical expected from the video signal. The clock generator will be described in more clotal before. The column selector is composed at a shift register (ort chown) heaving stages equal in ramber to the rumber of columns in the pixel error 102. The outputs of the stages of the shift register or connected via control fives in column order to the control incuts of the single stages of the shift register is connected via the output 141, of the first stage of the shift register is connected via the control incuts of the sempling decut; 152. For example, the output 141, of the first stage of the shift register is connected via the control input of the SNH directivity, of the simpling decut;

we coupt in style are staged on the soft register is connected with an earnyfing detail.

DOSO) The brailing edge of the horizontal sync agree or the horizontal between global clother is specially the control identifying digal (seeks the shift) register concidently the column selector (40 so that the the stage, whose output 141; is connected to the control line 139), is set to its 1 state, and the outpute of all the color is stage, whose output 141; is connected to the control line 139), is set to its 1 state, and the outpute of all the color stages are set to that of between The, the chock eighted PUKEI, progressively strike the 1 state atong the shall register of the plots and a state output of each stage of the shall register of the plots and the form connected by the stage is set the state that reconstruction the horse of the stage is

Eval register of the potent rate. As the output of each stages of the stiff register dranges form it to i, the same ple output O of the SM drout contracted by the steps is set to a value that represents the board of the whole og-rat corrected to the signal stoud Sof the SM drout. For earmple, as the bought if i, of the feature output of the stiff register dranges from 1 to 0, the earmple output of the stiff register dranges from 1 to 0, the earmple output of the stiff register dranges from 1 to 0, the earmple output of the stiff register dranges from 1 to 0, the stranges of the stiff register dranges from 1 to 0, the stranger output of the SM drout it SQs, is eat to a value that the year output of the SM drout in the surface output of the SM drout in the surface output of the sM so control input to the SM drout dranges statis, or the prack or mean, or RMS taked of the video drout dranges statis, or the prack or mean, or RMS taked of the sM drout from the corrupt of the SM drout may be set to some other level related to the SM drout may be set to some other level related to the

odeo eignal during the fine that the control input is in its 1 state, depending on the sampling characteristics of the SM sinute.

Fig. 1 The structure of the row exclector 134 is similar for the far outputs no stocker. 144. The number of stages in the stiff register fleat constitutes the row sciency for its equal to the number of some in the pixel stary 102. The row scienciar rocchers flor chock agona LINE from the chock agonal LINE from the chock by the training edge of the vertical sync signal and is chocked by the from mid chock agonal. The new science is the chocker and the vertical sync signal and is eddered as to chocker and the science agonal synchronic signal and signal and she wide oblights.

\$000.2] The dock generator 14.2 receives the video signature the video logar in the second signed in the station of the spatial logar modistor 100, the samp generator 142 will not be LED other 67. But of the pre-entre see known in the st and so the dock generator 142 will not be disconded in detail here. The dock generator less will not be outried signals SEL, CLE, ILLUM and BAL via the bus \$112 for dischtuden to the enabling drive discuss in the plate arms 102.

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post array 102.
[Bib57] As part of its dock and control signal generafor, the dock generator 142 curracts the vortical and
the dock generator 142 curracts the vortical set.
The found agnet signals from the video signal. If the
42. I video eignal techs such spressions is a book generator darwas syre signals from such attentiative incidia of
the start of the frames and fines of the video signal as
the start of the frames and fines of the video signal as.
Has

· ths.

\*\* (D064) The LED driver 67 receives a control signal from the clock generator 142 and crives the LEDs 69-71 (Figure 1) in response to the control signal to cause the LEDs to Burnineto the spatial fight modulator 100. The transprint signal control signal spatial for the first gradiest from the drive signal applied to 40. The transprint signal security disputes the drive signal applied to 40. The LEDs and the control dispute applied to the spatial fight modulators will be described below.

(10063) For each hame of the video signal, the ramp generator 144 generates two successive amp dignals, generator 144 generates two successive amp dignals, and hamper of the ramp denerates the first interpretate the reacond ramp signal in response to the halfing order of the verification by the carmp dignals are dignates the second ramp signal in response to the first ramp signals are dignited as having fines signal in response to the carm signals are dignited as having fines signals in the end of the first ramp signals are preferably inchliness since a non-finest stope provides simple and effective garma correction. Garma correction is required to correct far the non-finest perception of the appears thightness of the pixel by the human eye.

[0055] A suitable non-threar ramp signal may be genviatabol using a mamony. Values that define the level of the ramp signal at times corresponding to each cycle of a clock signal, such as a clock signal obtained by divid-

Ing the pixel clock signal, are stored in the memory. The memory is first clocked with the clock signal, and the generating a sultable non-linear ramp signal by digital or employ means are known in the art. The ramp generator verted to an analog ramp signal. Other tachniques for leads the ramp signals via the bus 113 to the pixel array auccessive volues read out from the memory are con-102 for distribution to the analog drive charits of the place els in the errey.

10067] The ramp signals generated by the ramp gen-erator 144 ere shown in Figure 7D and 11J below as beginning in a low clabs and increasing towards a high state. However, this is not oritical. The name aignets may Moreover, the rump signal may begin in the low state begin in a high state and decrease towards a low state. tion period and may then decrease towards the low and increase towards the high state during the Illuminastato in the following belance period, or vice versa.

A first embodiment of the enalog drive grount seconding to the invention of each of the pixels of the physi amay 102 is chown in Figure 4B. The anabog drive plary analog drive circuit 114 of the exemplary pixel 112 second row of the pixel array. The enalog drive circuits of the other pixels of the pixel erray are identical, but shown in Figure 4A. This pixel is the second pixel of the each is corrected to a different contrination of column circuits will be described with reference to the exem-

During each frame of the video signal, the arebus and row selector bus.

log drive circuit 114 receives on analog sample derived from the video signal, generales a drive signal in response to the enables sample and explice the drive can be regarded as being composed of the sample (0070) This embadiment of the analog of the circuit 114 signal to the pixel electrode 118.

the column bus 181<sub>2</sub> and states the analog sample. The drive signal generator generators the drive signal and applies the drive signal and applies the drive cignal to the pixel electrode 118. sample for the pixel from among the analog camples on The sumple selection section 128 will now be described. The sample selection vection selects and be displayed by the pixel 112 from the arrabg samples solociton section 126 and the drive signal generator 128. The sample selection section selects the analog stores the analog samples of the video signal that are to 132. The sample selection conton also leads the stored placed on the column bus 131<sub>2</sub> by the sampling circuit

The sample input 150 of the analog office circuit 114 is connected to the column bus 1312. Also connected to the sample input is the drain of the semple The gate of the sample select transister is connected via the row select input 110 to the raw select bus 133, connected to all the pinels electrods of the sample storags capacitor is connected of the cample select transistor is corrected to one elecrode of the sample storage capacitor 154. The other enakog semples to the drive argual generator 1239. (0072) The sample input 150 of the aradog drive o select transistor 152,

158. The gate of the sample output translator is con-nacted to the sample output control signal SEL gene-elled by the clock generator 142 and disatrouled by the sample output bus 158 to the gates of the sample output transistions of the analog of the circuits of all the pixels 154 and the sample select transistor 152 is connected to the source of the sample output transistor The node between the sample storage capac to a constant voltage source, e.g., ground. constituting the pixel array 102.

The drive signal generator 128 will now be 160. The electrode 161 of the ramp capacitor is connocted to the RAMP signal generated by the ramp grantering of the ramp grantering of the ramp grantering of the ramp grantering of the ramp has grantering of the ramp has described. The drain of the sample output translator 158 is comnected to the electrode 159 of the ramp capacitor 162 to the ramp capacitors of the enalog drive chours of all the pixels constituting the pixel array 102.

10075) The electrode 159 of the ramp capacitor 160 is nected to the reset control eignal QLE generated by the dockgonerator 142 and distributed by the reset bus 188 The inverter 166 is composed of the PMOS another and to the output of the Inverter, and the sources of which are nespectively connected to high and also corrected to the drain of the reset translistor 164 and the Input of the Inverser 166. The source of the reset transistor is commeded to a constant voltage source. a.g., ground. The gate of the recet transistor is conto the gates of the nesst translators of the analog offer transistor 170 and the NMOS transistor 172, the gates of which are connected to one another and to the laput of the invertor, the drains of which are connected to one tow constant voltage levels V+ and V. These constant voltage lavels may be, for example, the positive power drauts of all the pixels constituting the pixel anay 102. 90 8 8

0077] The culput of the invarior 166 is connected to mination selector transistor 176. The structure of the inverter 174 is identical to the inverter 166 and so will 178. The drains of the solocitor translators 176 and 178 dature 178 and 178 are respectively connected to the ILLAM control signal and the BAL control signal. The LLUM and BAL control signals are generated by the he input of the inverter 174 and to the source of the illunot be described. The output of the Inverter 174 is connected to the source of the balance selector transistor re corrected to one another and, by the conductor 120, to the electrode 118. The gates of the selector tran-160 and 182, respectively, to the gates of the selector transistors of the analog drive circuits of all the phots clock generator 142 and are distributed by the busses supply and ground, respectively. ŝ

The common electrode 33 shown in Figure 2B course V+/2 approximately mid-way between the high and low con constant voltage ş stant voltage sources. connected to

Operation of the just-described embodiment of he spetial light modulator 100 according to the inven-

ton will now be docated with reference to Figures 4A and 48, and the fining dapters shown in Figures 5A-87, and 64-68 and 7A-73.

Figure 5A shows the basic operation of the above-described embodiment of the spatial light modu-lator in which analog samples of frame 1 are loaded during the picture ported of trame 1, and a display ples of frame 1 during the picture period of trams 2. The ranses of the video signal are each divided into a varical blanking period VB and a picture period. During the picture period of frame 1, an analog sample derived coeration is performed in response to the analog semfrom frame 1 of the video signel is loaded into the sem-ple charge expector 154 of the snalog drive droug of coort pived in the placel array 102. This process will be Shullaneously, a display operation is performed in sample of frame 1 stored in the sample storage response to the enalog eamples of the previous trame 0. During the vertical bianking period of frame 2, the for of the pixel. Then, during the picture period of frame capacitor of each pixel is transferred to the ramp capac-2, a display operation is parlumed in response to the aredog sample transferred to the ramp capacitor of each pixel in the pixel array. Simultaneously, an analog cample of frume 2 is loaded into the sample stongs capacbatow with reference to Figures 6A-6R anabo

the LED driver 67 feeds current to the LEDe 69-71 to The waveform of the current supplied to the shown in Figures 58. During each illumination period, signal that they epply to their respective pixal destractes to cause the pixel to modulate the Intensity of the light 69-71 by the LED othor 67 is schematically cause the LEDs to itaminate the spatial light modulator 100. During the balance period following the illumination period and the vertical blanking period preceding the Burnination poriod, the LED offiver turns the LEDs OFF. Dufing the illumination period, the analog of the circuits of all the pixets constituting the pixel anay 102 similargenerate the illumination sequence of the drive reflected by the pixel. During each balance period, in which the spatial light modulator to not filuminated, the orating drive draults of all the phoets simultaneously generate the balance conserve of the drive signal. The balunce sequence of the drive signal is complementary to of the drive signal and estones the DC balance of the pixel. The office signal will be further described below with relevance to Figures he illumination sequence hor of the pixel. ű

goals. The waveforms of the LLLM and BAL control signals are shown in Figures 8C and 5D, respectively. During the vertical thanking period at the beginning of each freme period, the clock generable 142 generalise both of these control signals in fine 0 state. Accordingly, both the solution verticities a 7D and 17B are 0.FF, and 19 weltage on the pixel electrods 118 is approximately equal to the voltage on the common electrod 33 (Figure 25). The clock generator 142 generates the ILLIAM.

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control signal in the 1 state wherever the LED driver 67 supplies current to the LEDs 69-71. The ILLIM control signal turns the Illumination selector transition 176 CM, which connects the electrode 118 to the cuptor of the which connects the electrode 118 to the cuptor of the LED driver supplies no current to the LEDs, and the clock generalize generalize the BM. control signal shown in Figure 20 In its 1 state. This turns the beliance selection transists 178 CM, wider connects the electrode 118 to the output of the liversite 174.

with relevance to Figures 44, 48 and 64-67. Figures 64-60 respondively show the control signal waveforms on the control lines 1391-1389, corrected to the control lines 1391-1389, 1382, during the picture of the SM circuits 1389, 1382, during the picture (DDS3) The process by which an analog sample of the period of one frame of the video signal. Figure 6E shows an example of the waveform of the video signal frame of the video signel is loaded into the sample ctor. age aspacian 154 of the englog drive circuit at each pixel in the pixel amay 102 will now be described below Ye fed from the butter amplifier 188 to the signal inputs of the SAH circuits 1384-1384. Figures 67-63 respectively show the sample outputs of the SH clrudes 198,-138, fed to the column busses 1311-1314, respectively. In particular, Figure 6G shows the sample waveform on The column bus 131<sub>2</sub> connected to the sample input 150 tol signal on the control line 13% returns to its 0 sets, the SIH drouit 13% holds the leval on the column bus of the arralog drive circuit 114 of the pixel 112. Sempling begins when the control signal on the control line 139, good to its 1 state. When the control signal is in this state the output of the SAH circuit 138, connected to the column bus 1312 follows the waveform of the condifoned vidoo signal shown in Figure GE. When the can-131<sub>2</sub> at the level of the conditioned video signal at the tersition of the control signal. The lavel on the column bus remains at this level unall the next time the control signal on the control line 139, goes to its 1 state 14-way along the next line of the conditioned video signal. R Ŗ

along the mad the of the conditioned video signal.

[BOB4] Figures BL-fild show the wareforms of the control signals on the row select busses 1584, 1584, nespectively. Each of the control signals is shown as blanks to the district of one like of the video signals and is in its 0 state for the rest of the frame. However, the row select corticl signals may switch to their 1 states at a time later from the start of their respectives.

forces of Figures 6D-6R respectively show the waveforms on the sample starge expectations of the analog of Mote details of the pixels 184, 112, 185 and 188 in the second row of the pixels 184, 112, 185 and 188 in the second row of the pixels 184, 184 gramples of the second line of the video signal are accepted by these pixels. During the second line of the video signal, the carried signal on the row select but 134, corrected is to the pixel 112 bit the 1 state. The control signal furns the sample select transferr 122. CN, which connects the cample strange expector 154 to the sample input 130. As a result, the vidtage on fire sample storage

PAGE 13/79 \* RCVD AT 10/27/2006 3:15:30 PM [Eastern Daylight Time] \* SVR:USPTO-EFXRF-3/7 \* DNIS:2738300 \* CSID:7035185499 \* DURATION (mm-ss):35-06

Fitally, the voltage on the serrote sprage capacitor contros a constant level conresponding to the level had by the output of the SN4 chould 1885, at the end of the second quentar of the second fine. The votage on the sample strage capacitor medies this condition at the sample strage capacitor medies this condition at the [DGS5] In parlicular, as shown in Figure 69 when the control degral on the row select but 1532, chainges to its 1 state at the beginning of the second line, the writage on the serratio storage capacitor 154 of the serang drive. column bus 181<sub>2</sub>. These voltage charges occur as a rocall of the EA1 aireaf 130<sub>2</sub> sampling the second quarter of the second fine of the conditioned wideo signal. orault 114 charges to the level on the column bus 131<sub>2</sub>. The voltage on the sample storage capacitor then fol-lows the voltage changes, shown in Figure 6Q, on the the of the falling edge of the control varietims shown in Fours 68

Figures 60, 60 and 6R show how the voltages un the sample storage capacitors of the ploofs 194-166

ple atmose expector 164 from the sample struct 150, As a result, the voltage on the sample structge expector remains fixed at the lowel it heat when the control signal on the row selector has dranged state, as shown in Figure 6f. The voltages on the sample strange expectors. in the second row of the array takew the changes in the respeciest, when the control cignal on the now selector but 1332 (shown in Figure 810) is in its 1 sand, and femal contaut during the other three lines of the control eignal on the row selector bus turns the sample select translator 132 OFF, which disconnects the samvoltage on the column busses 131, 131g and 131g. nal, the control signal on the row selector bus 139, changes from the 1 state to the 0 state. In this state, the At the end of the second line of the video sigin the plasts 104-186 in the second row of the array also become fixed when the control signal on the row salocfor bus 1332 roverts to the 0 ctate.

the control signal on the one of the row select busses During the other three lines of the video signal, 133<sub>9</sub> and 133<sub>4</sub> corresponding to the line of the video signed recolved at the video input changes to the 1 stats. As a result, the voltages on the sample sample sample capacitors of the phods in the corresponding row of the phas array follow the voltage levels appearing on the column busses 131 r 131. At the end of each line of the causes the voltages stored in the sample storage apacitors of the ploads in the row to remain fixed units ing row of the pool erray reverts to the O state. This video signal, the control signal on the one of the row soled busses 130 r-193, connected to the correspond The processos by which the office signal genthe corresponding line of the next frame. [1000] The processes by which the deä

period and the training period constituting the trame 1 digitally period shown in Figure SA, but with a different time scale from that of Figures SA-SD. to Figures 7A-7G and Figure 4B. The drive signal has a cample and subsequently restores the DC belance of during the vertical blanking period and the illumination 1 state charation that depends on the value of the analog the pickel. Figures 7A-7G show the events that occur

signeds are in their 0 states, so both selector transistors 178 and 178 are OFF. Consequently, the voltage on the [0091] Figure 7A echamatically shows the waveform of the cument through the LEDs 69-71. During the variety common electrods 33 (Figure 28). At the start of the vertical blanking period VB, the reset signal shown in Figure 78 briefly turns the reset transistor 154 ON. The cal blanking period prior to the illumination period, no current flows through the LEDs, as shown in Figure 7A, the output of the ramp generator is in its minimum state, as shown in Figure 70, and both the ILLUM and BAL pibel electrode 118 is approximately equal to that on the reset transistor discharges the analog sample of frame O from the ramp capacitor 160, as shown at 187 in Figure 7E. The ramp capacitor is now ready to receive charge from the sample storage capacitor. 22 8 ĸ

the output select control agreal SEL shown in Figure 7C evitches the sample output hansistor 166 CNL This connocts the sample ecoage capacitor 154 in perallel with the ramp capacitor 164 which is in a discharged state. switches the sample cutout transletor OFF et or before the end of the vertical blastwing period, as shown in Fig-ure 7G. This isolates the ramp capactor from the sam-[DGBZ] After the reset transistor 164 has turned OFF, Cherge sharing occurs, and the vollage on the ranp ospacion rapiday increases, as shown at 188 in Figure 7E. The voltage level to which the voltage on the ramp expedien rises is proportional to the charge in the cample storage capacitor before it was connected to the ramp capacitor. The output select control signal SEL ple storage capecitor. 8 Ŋ

(1093) Notwithstanding the increased voltage on the ramp capacitor as a result of the charge sharing, the voltage on the electrode 159 of the remp capacitor: 160 is below the threshold voltage of the invarter 166 at the end of the vertical blanking period. The threshold voltthe output voltage of the inverter 166 continues in its high state, as shown in Figure 7F. However, since the pixel electrode 118 is disconnected from the outputs of both inverters 168 and 174, the voltage on the pixal electrode 118 is approximately equal to first applied to age is indicated by the line 189 in Figure 7E. As a result, \$

verball blanking period VR. In response to the trailing edge of the vertical sync putse marking the sclart of the filmination period, the clock generator 142 ceuses the

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LED drives 67 to feed current through fine LEDs 68-71
ses shown in Figure 7A, east the ILLIM control signal to
the bit state, and vitgoes the nump powerbor 144 to
curring and state and vitgoes the nump powerbor 144 to
the state of the number of the numbe

(DOSE) The ramp signal generated by the many generated 14 is explicate to the electrode 161 of the emporator 160. As the first temporal portion progresses, the ramp signal causes the voltage on the electrode 193 of the ramp capacitor to increase the voltage on the electrode 193 of the ramp capacitor to increase in sigh with the ramp signal causes the voltage on the electrode 193. He voltage on the electrode 193, the voltage on the electrode 193 is about at 192 in Figure 17. Show the point 193, and the output of the inverter changes to the factor, as shown at 192 in Figure 17. Show the prior electrode 119 is connected to the output of the inverter provide on the electrode 193 is connected to the output of the inverter provide output of the latent provided to the low state, as shown in Figure 78. This make the end of the litter language on the electrode 193 of the econd temporal portion of the illumination perior. The part electrode connection of the illumination perior flows of the latent and on the end of the illumination newhold remains.

nation period. The piral electrochormanis in the details of the scord through period constraint in the remains of the the scord through period chown in Figure 7A.

100977. At the end of the liturihation period, ramp signed that fossits, as shown in Figure 7D, and the voltage on the electrods, as thown in Figure 7D, and the voltage on the electrods as both in any experior tale quickly the level before the threshold voltage of the herener 188. So This causes the output of the invester 188 to resert the stalls, as shown at 193 in Figure 7F. In addition, both the little control signed and the BAL cured dignal charge state, as shown in Figures 5C and 50, respectively filts than 8 ellumination electror translater 178 ON, which trainfers the controlled in the operator did in worster 174. The output of the invester 168 to the output of the invester 168 to the 1 state. Accord as 100, during the less than 199. In the 1 state. Accord as 100, the bigger of the place lessands remains in the 0 state as shown in Figure 3C.

(1099) When the lavel of the electrode 159 of the ramp capeabor reachos the firsthold vallage 188 of the inverter 168 orders more, the outputs of the inverter 169 changes state, as shown an 199 in Figure AT. The output of the inverter 174 changes state, as a result of the inverter 174 changes change to the pixel electrode 118 changes from the 0 state to the 1 state, as shown in Figure 7C. This marks the end of the first temporal portion and the beginning of the second temporal portion of the loanness perfod. The votinge on the place electrode remains in the

1 state for the exocond temporal profice that constitutes the fermanister of the balance pendent shown in Figure 7A (2009). The rarry waxdom returns to its maintain state at the end of the balance pende, and its execution at shown in Figure 7B once more turns the reset transferor in Figure 7B once more turns the reset transferor in Figure 7B once more turns the reset transferor in The BAL control signal remains in its 0 state and the LLUM composition from the 18 0 state and the LLUM composition from the 18 0 state and the LLUM composition for the balance period. The plans state of the BAL control signal states for the plansferor period. The plansferor is the 18 form the inventers once mone, as shown in Figure 7Q.

(010) During the balance period, the drive signal has is in that service that is an orderneatary to the resental emparal portion that is a complementary to the first temporal portion in which the drive signal applied to the pide electricia when the sprietal state during the Burninston period when the sprietal it is that during the Burninston period when the sprietal it is not happed electrode 118 is set to that 1 state and age on the pide electrode 118 is set to that 1 state and 20 to the 0 state and portions of the display period so that the DC betance of the topic significant.

Fati the DC betance of the pixel is maintained.

[IIII] The duration of the fixel temporal portion of the lithmation peaked in which the pixel decarded 118 remains in the 1 state depends on the singly voltage to 35 which the north capacitor 160 was decayed by change statution with the sample atmosp expeditor 154. The DC bed and obtained on the historial peaked in the treation with the harden capacitor 155. The DC bed and obtained and the historial decay of the interpret by the obtained of the results of the historial and the threating which object of the result and the threative 160 changes state almost him of the threative 160 changes state almost him modalely when the vitrage of the analysis of the sando stange stange organize companies to the meantum of the operation period of the wideo signet. On the other hand, the inverter closs not widen the sample voltage is set the minimum of the dynamic range of the vitrage of the dynamic range of the vitrage of the dynamic range of the vitrage is set the minimum of the dynamic range of the vitrage of the minimum of the dynamic range of the vitrage size at

dynamic range of the victor signal.

(Drict) The broken lines 166 and 197 in Figures 77 and 70 factors the broken lines 166 and 169 in Figures 75 and 76 factors the broken during of the page described 189 cutput of the investrat 166 and the page described 189 responsively, when the level of the analog sample is lower, as inflacted by the broken fine 156 in Figure 7E. The orgally-broyer duration of the 0 state of the potential efforcing behavior period is inflated by the broken the 198 in Figure 7D.

of the broken the 198 in Figure 7G.

[UKIG] in the stone-described enthochrent of the aready drive circus, and in the enthodinaries to be described below, the stopes that drive the plant elso trode are required to change state only two por theme. The aready drive droughtes a tower construption then a eligible drive droughtes a tower construption then a eligible drive droughtes a tower construption than a eligible drive droughters as tower drives only remade grind drive droughters as the standard grind drive droughters are disconting as department on the suitability aspead of the electromagnets of the electromagnets of the standard drive droughters are described and the suitability of the suitability between the furnism of the first temporal portion of the drive elginal applied to the pixel.

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electrodo 118 curing the Burnization period and the antido cample source in the sample storage coperator. 154 deports on the investor 164 deports on the investor 165. The three-bod voltage is process-deportion, and can offer between relate, between post arrays on the come weley, and between the analog diverciously fectuated come weley, and between the analog diverciously in the same post airay. With current processing fectuatology, showe threshold virges variations mit the groy-scale resolution of the spatial light incubators to be should four biss. Mass (prepries and video applications require a reproper group of the post of the processing sequences.)

analog figure 8 shows a second embodiment of an analog offive droug fact motions the effect of threshold working waterfaces, and that can threshon provide a ground greate greate recording in this embodiment shown in Figure 8, elements beto correspond to those of the embodiment shown in Figure 48 are indicated by the surhodiment shown in Figure 48 are indicated by the south-order entiments, and will not be described egain from The semple derivation and distribution city cut that provides auxiliary send control eigents to all the provides auxiliary send control eigents to the orthodiment shown in Figure 8 is entitler to that shown in Figure 8 is entitler to that

intern.

(1916) In the embodiment of the analog drive circuit shown in Figure 8, the empodiment shown 129 is the same as first of the embodiment shown in Figure 48. In the drive shorel generator 129, the trput of the inverter 169 is connected to the electrode 159 of the inverter 169 is connected to the electrode 159 of the inverter 169 is connected to the electrode 159 of the carried approach 203 whose drain end source are connection transistor 203 whose drain end source are connected to the leptul and output, respectively of the inverter 168. The gate at the offset connection control signed ORC CORR. The offset connection control signed ORC CORR. The offset connection control signed IS

by the clock generator 142 and is clarifuled by the bus
205 but in gates of the offset correction transitures of
the areage drive circuits of all the plates constituting the
plate array 102.
[6/107] Firedly, the source of the reset transistur 164 is
corrected to the netherous signed SOLEAT. This released serious is generated by the obod generator 142 and
is discharted by the bus 211 to the cources of the reset
transisture of the serion drive circuits of all the plates
correlating the parel array 102. As shown in Figure 9C,
the references agree ISCLEAT has two retices, a high
sistem Virge equal to the desired freshold vicilise of the
inverter 166 and a low state dose to the low voilege
flowd Vir. In one practicel emboriment, the high state of
the reference signed SOLEAT was hardway between
thigh and low voileges Vy and Vy.

[PI'08] Operation of the entrodiment shown in Figure 8 is similar to that of the entrodiment shown in Figure 48. Hewer, at the bughinthy of the vortical brafking protect VIB of each frame, the offset correction contridety OF CO. COAR and the clear control signal CLE are issued as shown in Figures 9A and 9R, respectively, in addition, the relevance signal SCLEAR endates in its addition, the relevance signal SCLEAR endates in the

Myh dathe V<sub>RES</sub> at the beginning of the vertical blanking period, as shown in Figure 9C. The orders correction corruit signed terms ON the officer correction transists 28G, which Inferonments the input and output of the Investor 16G. Correcting the output of the Investor to its Plus death or Stage on the input of the Investor to its Plus death or Stage on the input of the investor when electrode 207 of the coupling capacitive 201, precisely to the threstorial values of the investor. The clear counts signed CLE turns the receipt transister is the receipt transister or corrects the clearched 209 of the coupling capacities 201 to the reserves against SCLE-RI in its high statu. The reset turnish or signed SCLE-RI in its high statu. The reset turnish the addition of the consideration reasister together set the voltage narroes the coupling capacities 201 to a walue equal to the investor between the actual threshold voltage of the Investor and the desired threshold voltage. Vers.

19109] Partway through the vertical blanking period VR, the corms depend OS CORR is deseasand, as shown in Figure 8B. This turns the offset correction team sizes 280 OFF, but the votinge excess the coupling capacity 201 nemales. Simultaneously, or slightly leave, the reference signal SCLEAR evelucies to lis but state V, as shown in Figure 9C. Sixon the count of signal QLE is all deseated and the need tearistic 164 is 618 QM, the ramp capacitar 160 discharges to as low voltage state through the resed learsistic. After a time sufficient for the nemy expenditor to discharge thin, the countral signal QLE is de-assected and the resed transistor. 164 is de-assected and the resed transistor 164 in the transition for the nemy expenditor to discharge thing the countral signal.

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but soft.

(D110) Aher the result rensistar 164 has turned off, the control egral SEL is asserted, as shown in Flyue 9D. This turns the selector harraktor 159 ONL Charge share in the Demonstrate as expected above with reference to Flyue 7E. The control agains SEL is dues earted before the end of the vertical blanking period VB is factor.

O (1) 11 Coeration of the other signal generating excion during the illumination and believe pariotic constitution.

The display period is the came as that described above with reference to the plants PT-70. When the ramp wait eage is applied to the electrode 161 of the ramp capacity.

The bearter 168 will tramps state when the voltage on the electrode 159 of the namp capacitor readness on the electrode 159 of the namp capacitor readness of the inverter 168. The searce will be true for the invertex of the invertex 168. The searce will be true for the invertex of the invertex of the invertex 168 in the size of the invertex 168 increases the grey coale resolution of the embodinent of the applied light invokaletar excending to the invertion to greater than search the same of the invertion to greater than invokaletar excending to the invertion to greater than search the same of the than the capacital light invokaletar excending to the invertion to greater than search the same of the same of

(0112) The embodinest of the analog drive droublius described with reference to Figure 8 includes three expections. The area of efficien coordinal by those

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especies using present-day charteston techniques requesions are acted in the area of each arriag drive chart, and finite the number of pues final can be provided on a die of a given size. Mos, the speals light modulator is illuminated for a total of one had of the pairs. It was period of the video signal. Since the various barrietty period of the video signal. Since the various barrietty period is about 4%, it would be ordered afterney of the world light modulator is then 4%. It would be ordered by the ordered light modulator to the theoretical maximum of 19 CMs and to reduce the maximum of 19 CMs and to reduce the maximum of 19 CMs and to reduce the number of capacitars to the per arrabo of the direct.

dort 18. A second embodiment 214 of the unalog drive dord according to the investion will be described need with reference to Figures 104 and 108. This embodiment general standing last discount of the part of t

space 1978 inconsistor having a greater number of poses on a given die size fran the entrodiments stronn in Tiguros 48 and 8.
[0114] Figure 10A strons the sample derivation and
distributor tiend. 204 that derives enablog samples from
the video digral received via the video frout 106 and
then video digral received via the video frout 106 and
the video digral received via the video frout 106 and
the video digral received to the analog differ circle to
the pixels consisting the pixel among the cruits of a
the pixels consisting the pixel among the cameral the
analog differ of circle 204 fest correspond to the sample derivation and distribution circle 104 shown in Fig.
ure 4A are indicated by the same reference numerals
and will not the camer electron currents with 100
odd/od. The sample derivation and distribution death of
tinciance by the same reference numerals
and will not the consorbed. Elements fest are sinder are
indicated by the same reference numerals
and will not the cameral reference or numeral with 100
odd/od. The sample derivation and distribution death of
time bedection but and an event-finine
selection but a for and therefore the integers
distribution that is and now of pixels in the pixel among
[0116]. As will be described in more destall below with as

Selection tax for each new of plads in the pixel emp.
[Utig] we will be descabed in more death below with
reformers to Figure 108, the endog drive chould 2014 of
the exemplary pixel 212 in the plad array 202 has a
sample trout, add-hame and even-frame now select
liptus, a many bright, and and even sample each
liptus, a many bright, and and even sample each
liptus, and a comparative sense control truit. The analigidities and a comparative sense control truit. The analigidities and a comparative sense control truit. The sample
consisting the pixels have as similar. The sample
consisting the pixels have bed nothron of the pixel array
are connected to a respective column but which is connected a respective output of the sampling closul 192.
For countries, the sample inputs in the first
column of the pixel array are connected to the column

bus 1314. The location in each line of the video signal from which the analog sample received by each column of pixels is derived depends on the row position of the column in the pixel saray 202.

s (0116) The add-frame row select inputs of all the pixels it each row of the pixel army 202 are corrected to a respective ordinaries row select broats of all the pixels in each row of the pixels in each row of the pixels in second control or respective even-frame for the pixels in the second row of the pixels in the second row of the pixel in within the pixel 212 is located are connected to the odd-frame row select broats of the own-frame row select pixels of the pixels in the second row on the row select broats of second row on the connected to the odd-frame row select bus 1985.

(917) The other and eventrame tow elect buscass are commerced to respective outputs of the oddieven farms selector 234. The oddieven frams selector has one town the the text from outputs corresponding to each row of the brighted start from outputs corresponding to each row of the oddieven frams elector. For example the row selector 134 to a corresponding toput of the outputs of the tow selector in the 183, commercis the second output of the row selector in the 183, commercis the second output of the row selector in the 183, output of the outbuts commercia from selector commercia to the outputs corrected to the outbut of the row selector in the 183 and 1815. An analog given of the row selector the search selector commercial to the outputs corrected to the outbut commercial to the row select fruits is the 1 state, for occurred to the video dignal, the row select fruits is the 1 state, for occurred to the selector of the first of the row and the text selector of the selector of scath frame of the video signal use received these of scath frame of the video signal use received these of scath frame of the video signal use received these

pti (g) The oddleren trans selectra 235 is composed of a pair of two-trput gates for each row of ptets. The odput of the off the gates connected by model of the odd-row 1350, of the row und the output of the other of the gates is connected to the aven-frame select bus 1350, of the row under of the pates is connected to the own-each bus 135, of the row, where it he has now number. A first trout of each of the gates connected to the own-each bus 135, of ornegoning to the row of phase. The second input of one of the pates is connected to the own-each bus 135. The offer that of the own-frame control to the own-frame control to second input of own-frame or the own-frame so control bus 239. The own-frame so control bus 239. The odd-frame and con-frame control signals in the 1 tests, for earning during odd-runbered frames of the video signal and is in the losses during even-numbered frames on-

(0119) With the emengement just described, the odd/oven frame selector 235 maintains in the 0 state the

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out- and even-trame row edect busess of all muss except the row whose now select livel is in the fishs. The states of odd-forme row select bus and the sever-trame row select bus and the sever-trame row select bus of the sever-trame row select bus of the sever-trame row select bus in the sever-trame row color trames control is up in the fishs follow the state of the odd-trame row select bus is in the fishs and the even-frame row select bus is in the fishs of whom the odd-frame row select bus is in the fishs and the even-frame row select bus is in the fishs and the even-frame row select bus is in the fishs and the even-frame row select bus is in the fishs of which are decreased only which the even-frame row select bus is in the fish to the fish the arradog draw sith reference to Figure 4B. However, the odd-trame surface of the video is signal to be stored in the odd-trame and even-trame series expetinely, of the analog shand confirms and even-trame series expets.

described with reference to Figure 108. The analog firms 2280 sample selection conton, the even-frame sample selection section 228E and the drive signal gon-erator 228. Both semple selection sections are composed of identical circuits whose operations are fare multiplicated to maximize the Municiplic cificiancy of the spalls flight modificate 100. One of those duplicate cir-The analog drive circuit 214 will now be plary pixel 212 shown in Figure 10A. The analog drive drauft can be regarded as being composed of the oddcuits receives an analog samplo of the ourrent frame of the video signal at the sume firm as the chive eignal generator generates a drive signal in response to an analog sample of the previous trame stored in the other. drive circuit 214 is the analog drive circuit of the exem-The cooking semple selection section 2260 selects an analog sample derived from each add frame stores this enoting sample in an even-frame storage of the video storal and stores the selected analog sam-ple in an odd-frame sample storage capegior, and the even-frame cample selection septon 226E selects an erelog sample derived from each even scane end capacitors are atternately selected and led to the drive signal genomics 228 which generates a chive agnal in erator sequentially generates ofthe signals in response capacitor. The analog samples stored in the storage to the analog samples derived from consecutive frames of the victoo signal. Each drive cignal generated by the other signal generator exclitionally restores the DC toxresponse to each entalog cample. The drive signal gen-(0210)

ance of the pixel 21:2.
[D122] The acch feature sample selection section 2260 of the carebo drive droud 214 of the exemptary paid 219 will now be described. The overlature sample selection section 224E is almost identical and will not be described. Corresponding tennets of the odd-forms sample selection section and the even-frame sample selection section and the even-frame sample selection section and the even-frame sample selection section south and the same increases numerate with the letters 0 and E, respectively, action.

214 is contracted to the column but 1319, Also connocted to the sample separate form of the sample select function 2200, the gain of which to comected with the odd row eated troud 2100 to the odd-frame row select but 1200. The source of the sample select transtant is connected to one electrode of the sample staforce capacitar 2540. The other electrode of the sample stander capacitar is corrected to a constant voltage lovel, eq., gount.

The node between the sample storage capas for 2540 and the source of the sample select transistor The gate of the carride output transistor is connected to for 242 and distributed by the even control bus 239 to because the odd-trame semple selection section 2260 2520 is also connected to the source of the saruple output transistor 2560. The drain of the sample output trandistor is connected to the Binput of the comparator 25% he control signal EVEN generated by the clock generahe gates of the earnple output translature of the coldframe sections of the analog of two circuits of all the plaels constituting the pixel array 202. The sample output feeds stared amilog samples to the drive signal section 228 at the same time as the even-frame sample section and storage section 228E receives an analog sample from the sample imput 250. For a similar reason, the ple selection section 228E is controlled by the control transistor 2580 is operated by the control signal EVEN cample output transistor 256E of the even-frame samsignal ODD distributed by the odd control bus 237. **10**(24)

Supera v.U. cozarotectory the God control total S.V.

[R123] The comfort signal EVEN is also convected to the gath of the ramp signal scaleon transistor 2570.

The source of the ramp signal scaleons transistor is connected to the ramp signal scaleons transistor is connected to the ramp signal RAMP percentably the ramp signal box 218 to the ramp signal selector transistors of the arrange drive afterilis of all the pixels constituting the pixel surface of the factor of the ramp signal selector transistors of the arrange drive afterilis of all the pixels constituting the pixel surface of the constituting the pixel surface of the connected to the Atput of the comparison 252.

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257E is corrected to the Birput of the comparator, and ment, areting samples derived from the even fields of log samples derived from the odd framee and stored in the sample storage capacitor 2540 are ted to the B The even-frame sample selection section 226E differs from the add-frame example selection section 255, the drain of the ramp signal sodector transistor the gatos of the transistons 256E and 257E are conthe video signal and stored in the comple storage hout of the comparator and the namp signal is fed to the 2360 only in that the drain of the sample output transfer tor 256E is connected to the A input of the comparator nected to the OOD control signal. With five arrange capacitor 254E are fed to the A input of the comparator and the ramp signel is fed to the Bingut, whereas ana-928 8

(0127) The drive signal generator 228 will now be doorbed. The drive signal generator includes the commercial 255. The comparator 255 is a switched-cense

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log samples of the eventrames. Frames 1 and 3 are odd section 225E and the office signal generator 228 on area 23 the state of the comparator comes control signel SENSE generated by the clock generator 242 and distributed by the comparator sense bus 260 to the comparators of all the places community the pixel amay 202. The compenstor sense control signal serves two functions. Flest, the constant detection sense with respect to the ramp signal and fine analog samples despite the abamation of comparator sense control signal inverts the detaction sense of the comparator in the Numbration periods of the detection some is evented and the output of the companion in a 1 state or a 0 state depending on whether the voltage on the B trout is greater than, or loss than, the voltage on the A input. Second, the comsuccessive frames. This provides the comparator with a the connections of the name count and the analog samples to the A and B inputs of the companion. For oddramo analog samples, the detection sense of the comparator is convenional, and the cutout of the companfor in a 1 state or a 0 state, depending on whether the votage on the A input is greater then, or less than, the vollage on the 8 Input. For even-frame analog eamples, illumination period. This enables the componator to generate the belience portion of the drive signal simply by parator sense control cignal invents the detection sense of the compensator in the balance period latewing each repeating of the cycle of the ramp signal connected to

(0128) Alternating the inputs of the comparator 255 to which the analog samples and the ramp signal are conratur reduces the visibility of errors resulting from differences in the input discol volleges of the comparafors. The inputs are attemated and the detaction sense of the comparator is inverted between consecutive over frame, the input offset adds to the ramp signal, so the pixel appears dinner then its normal brightness. The brighter appearance and the dinner appearance of the pixel average between the two frames, so that the nected and invaring the detection sense of the compatrames. For example, in an odd frame, the triput offises may add to the enalog semple so that the pixel appears brighter than its nominal brightness, in the following phod repeans et its nominal brightness. and of its inputs.

is smell, or the input offset voltages of the comparature similar, the analog drive circuit can be simplified. This to the Ainput, for exemple, of the comparator, and con-(0129) If the input officet voltage of the comparator 25.5 of all the analog drive circuits of the pixel array 102 are the waveform of the comparator sense control signal can be done by eliminating the ramp signal eclocitor landstors 2570 and 257E, connecting the ramp signal necting the drains of the sample output transistors 2580 and 256E to the Binput of the comparator, in this case, comparator is normal in the lifumination periods and should be changed so that the detection sense of the nverted in the balance periods.

The output of the compension 255 is connected to the pixel electrode 118 by the conductor 120.

cample and storage social 2550 and the drive signal generator 229 of the ambig drive chart on analog samples of the odd-numbered frames of the video signal. Figure 118 shows the operations sequentially performed by the eventrame sample selection storage. (0131) The drive signal generators shown in Figures 8 or 158 may be substituted for the drive signal generator [0132] Operation of the enetog drive circuit 214 of the searchery pixel 212 will now be described with referpixel 2.12 is located in the eacond column of the second row of the pixel erray 202. Figures 11A-11O show the maveforms in verticus parts of the carouit in the course of bading analog samples of three consecutive tramps 1, 2 and 3 of the video signal into the sample selection sections 2260 and 226E of the circuit, and generating drive signais in response to analog samples of the prethe operations sequentially performed by the odd-frame ence to Figures 10A, 10B and 11A-11Q. The exemplary vicus frame 0 and frames 1 and 2. Figure 11.A shown 228 shown in Figure 10B.

(0133) As shown in Figure 11A, during the frame 1 sample load parted, in which frame 1 is received at the vidoo lirput 106 (Figure 10A), an analog sample of frams 1 is loaded into the odd-frame sample selection LEDs 69-71. The drive signal of the LEDs is scheming-cally shown in Figure 11G. In the balance period of the frame 0 display period shown in Figure 118, the drive signal generator generates a drive signal that restores ure 118 is concurrent with the frame 1 cample load period. During the Burnington period of the frame 0 display period, the drive signal generator 228 of the circuit modulator 100 is illuminated with light generated by the ecotion 2260. The frame 0 display period shown in Fig. generatos a drivo signal in response to an analog egmple of the previous frame, frame 0, and the spettel light the DC balance of the pixel, and the spatial light modutrames, and frames 0 and 2 are oven frames. lator is not illuminated. 8

[M34] During the trame 2 cample load period shown in Figure 11B, in which trame 2 is received at the video irput 106 (Figure 10A), an analog sample of frame 2 is loaded into the even-dams sample selection section ng the Bumination period of the frame 1 display period, 220E. The frame 1 display period shown in Figure 11A generator generates a drive signal that restores the DC belance of the pixel, and the spatial fight modulator is is concurrent with the frame 2 semple load period. Durthe offive signal generator 220 generatas a drive signal in response to the analog comple of frame 1 stored in the odd sample selection section 2260, and the spatial ight modulator 100 is illuminated with Rolf generated by diplay period shown in Figure 11A, the drive signal no LEDs 69-71. In the balance period of the framo 8

Finally, during the frame 3 sample load period shown in Figure 11A, in which frame 3 is received at the 9135

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trains 8 is basted into the cod-frame sensyle salection section 2260. The frame 2 display period shown in Fig. ure 118 is concurrent with the frame 3 sample load 10A), an analog sample of period. During the illumination period of the frame 2 display period, the drive signal generator 228 generates a drive signal in nexponse to the analog comple of frame 2 stored in the even szample selection section 225E, and ated by the LEDs 69-71. In the balance period of the the special light modulator is illuminated with light generales a drive signal that rectores the DC belance of the pixel, as shown in Figure 11A, and the spatial light modframe 2 display ported, the drive styrial generator generulator is not illuminated.

Figures 11D and 11E show the states of the periods that the odd-numbered frames are received at ing the odd-trame sample load periods, i.e., during the elighty asymmetrical to prevent the translators controlled by these control etgnals belong ON annufamencusy and to prevent charge sharing between the exportures 000 and the control eignal EVEN, respectively. The control algnal ODD is in its 1 state dur-The video input 108, and is in its 0 state during the eventramo cample load perfods, i.e., the periods during which the even-numbered frames are received at the video input. The control agnets ODO and EVEN are 2540 and 254E as a result. 9486)

Adeo bignal, an analog sample of the frame is loaded (0137) In the sample load period of each teams of the nto the analog dive circuit 214 by processes similar to he amulog eamples from the cuts frames of the video sgnal are loaded into the odd-trans sample selection section 2260 of the aretog dive circle in response to the odd-famo row select signal. Figure 11F shows the els located in the socand row of the pixel array 202. The ple selection socions of the analog drive diruits of orty corresponds to the row select objust shown in Figure 68. However, as can be seen in Figure 11F, the oddhase described above with reference to Figures 6A-GR. odd-frame row select eignal ted via the odd-frame row select has 1330, to the analog drive charits of the pixodd-frams row select signal ceroco the odd-frame samthe pixels located in the second row to accept the enslog sortples from the column busees 1811-1314, and frame row select signal is only asserted during the sam-Figure 11G shows the even-frame row saled signal fed the phot array 202. The waveform of the even-framerow select signal is the same as that of the odditume row select signal shount in Figure 11F, detayed by one frame pie losd periods of the odd frames of the wideo signel. via the evon-frame now select bus 133E<sub>2</sub> to the enabo drive circuits of the pizets located in the second row of select exural is the same as

furtifier of one line of the video eignel, and is in its 0 Each of the row select control signals is shown in Riguros 11F and 11G as being in its 1 state for the state until the corresponding line of the next odd or enon-frame. Howover, the row solect control signals may 0158

switch to their 1 states at a time later than the start of Figure 11H shows how the voltage on the oddfame cample storage capacitor 2540 of the serging drive circuit 214 dranges during the sample load perfods of frames 1-3. Initially, the voltage on the sample storage capacitor corresponds to the analog sample of the beloe-previous framo (frame -1, en ood frame) of the video signal, as shown at 261. Then, the odd-barne row edect donal shown in Figure 11F is asserted during the second the of hame 1. This cignal causes he comple select translator 2520 to correct the sample storage solical translator to disconnect the sample storage capacitar from the column bus. The sample attrage apparator continues to hold a voltage corresponding to capacitor 2540 to the column bus 1312. After a delay corresponding to one pixel, the arabog sample come sponding to the second pixel of the socond line of the fame it is fed to the sample stonege capacitor. This causes the voltage on the expection to change to the select signal is de-essanted, which causes the sample lovel, as indicated at 263 in Figure 11H. After a datay corresponding to two more picels, the odd-frame ron the analog sample of frame 1 until the addressme now colect signal shown in Figure 11H is next asserted during feame 3. Then, the sample stonage capacition ecocpts en analog sample of frame 3, as shown at 265 in Figure 11H. ä

During the even frame sample load periods, the even-frame row select signal fed via the even-frame row select bus 1995; to the analog drive droubs of the pixobs located in the second row of the pixel array 202 is asserted, as shown in Figure 11G. The even-frame row edled signal causes the even-frame sample selection sections of the analog of the circuits of only the pixels bocated in the second row of the pixel enay to except changes during frames 1-3. Intially, the voltage on the sample stange capacition corresponds to the analog analog camples from the column busses 131,-1314. Ine of frame 2, as shown in Figure 11(3. This signal causes the sample select translator 252E to connect the cample storage capacitor 254E to the column bus 131<sub>2</sub>. setrate corresponding to the excord place of the second This causes the voltage on the capacitor to change to Figure 111 shows how the voltage on the sample stor capacitor 254E of the analog drive circuit 214 sample of the previous framo (framo 0, an even frame) of the video algral, as shown at 267. Then, the evenrame now select eignal is asserted during the second line of trame 2 is fed to the cample storage capacitor. one corresponding to the analog sample, as indicated at 269 in Figure 111. After a delay corresponding to two the column bus. The sample storage capacitor continues to hold the voltage corresponding to the analog Atter a delay corresponding to one pixel, the analog more pixels, the eventuame row select signal is deasserted, which causes the semple select transista ₹ 2 8

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through the rest of the sample load perfods of drive signal in response to the ending earnible of the pre-vious fearns loaded from one of the sample solicition socions 2260 and 226E during the sample bad period hames 2 and 9 until the oven-frame row salect eignal is the drive signal generator 228 generates the Figures 11J-11O show how, in each frame of the ramp signal RAMP; in the exemple shown, the the drawings, but a non-linear characteristic is pro-formed. A non-linear characteristic entation gamma con-rection to be porformed, as discussed above. The ramp of the previous frama. Figure 11J shows the waveform oqual to one-half of the frame period. A ramp signal with lifinour voltage time characteristic is shown to shapility critical. The ramp eignal may begin in a high state and dear sease towards a low state. Moreover, the ramp significant may begin in the low state and increase lowards the ramp signal has a sourboth waveform and has a perior high state during the filmination period and may then decrease towards the low state in the following betance signal is shown in Figure 11J as boginning in a low state and increasing towards a high state. However, this is not ned essented in the next even frame 4 (not shown). Or wice versa.

Figures 11K and 11L respectively show the vollage on the A and B inputs of the comparator 265. In addition, broken lines show the weretorms of the pordons of the ramp signal fed to the other input of the comshown in Figure 118, the control signal ODD shown in output transistor 236E and the ramp signal selector rancistor 257E ON. At the same time, the control signal and turns the sample output transistor 2560 and the ramp signal coloutor transistor 2570 OFF. Consehe comperator 255, as shown in Figure 11K. The remp perator. At the start of the frame 0 thuringion ported Figure 11D changes to its 1 state. This turns the sample EVEN changes to its 0 state, as shown in Figure 11E. the enalog eample of the previous frame 0 stored in the sample storage capacitor 254E of the even cample selection section is connected to the Airput of rains, se shown in Figure 111. The wevelorm of the ramp signal is elso shown as a broken line in Figure algnal RAMP is connected to the Birput of the compa-142

11.1.

19.13. Since the level on the A trout of the comparation is retailed, higher than that of the B trout, the morning outful of the comparator is a 1, as a shown at 271 in Fig. 10 in 11th. The comparator some control agrees STBVES allows in Figure 11th is in 1b 1 state, so the detection series of the comparator is normal end the other signal convexted to the pixel electrode 11th is in the 1 state for Convexted to the pixel electrode 11th is in the 1 state for Convexted to the pixel electrode 11th is in the 1 state for Convexted to the filter increase as the forme (2014). The camp signal PAMP increases as the forme 0 Elumination ported progresses. When the rarup signal

118, change from a 1 to a 0. This marks the end of the first territorial portion of the Burnington period. The Velocitodin centaris in the 8 state for the second temporal portion retennal 275 in Figure 110. The second temporal portion constitutes the remainder of the frame 0 this majoriton centalities the remainder of the frame 0 this majoriton period.

(0445) A the beginning of the frame 0 belance period shown in Figure 118, the level of the rarp signal RNAP shown in Figure 118 the level of the rarp signal RNAP shown in Figure 118 charges state. However, since the compenture sense control signal SRNSE also changes state, as shown in Figure 118 flow state for changes state, as shown in Figure 118 the sethal culture of the compensator remains underspect. Obresquently, the state of the pixel sleep from tenders from the remains underspect during the first temporal portion of the bullance period, as shown at 277 in Figure 119.

The ramp signal RAMP once more increases marks the end of the first temporal portion of the bal-ance period. The electrode remains in this state during as the frame 0 belance period progresses. When the camp signal stightly expects the voltage of the sample clonage capacitor 254E, the nominal output state of the rator sense control signal remains unchanged, the state of the pixel electrode also changes from 0 to 1. This fine secod temporal portion, a shown at 279 in Figure The spatial light modulator is not illuminated during the first and second temporal portions of the balance period comparator 255 changes from 0 to 1. Since the campa 110, constituting the remainder of the balance period. Stalance period. The states of the crive waveform in the are appeale to those in the first and second temporal portions, respectively, of the Munimation ported so that the DC balance of the pixel is restored. 8

19 LIV Death of the start of the terms is farmination period, the control signal EVDN shown in Figure 11E charges to the control stages. EVDN shown in Figure 11E charges to the control stages of the control stages of the search section coction 2560 and the search section section coction 2560 CM At the cock trans earthe selection section 2560 CM At the same time, the control strying single selection stages are shown in Figure 11D, which turns the sample output translater 2565 and the start posteral selection section 25E CMF. Consequently, the sample sample fon 25E CMF. Consequently, the sample sample of an author strained of the cod sample selection section, in which an author strained of selection section, in which an author strained of selection section, in which a capacitar of the comparator 255, as shown in Figure 11K. The samp signal selection in Figure 11K. The waveform of the comparator, as shown in Figure 11K. The waveform of the samp signal is also shown as a broken the figure 11K.

a vomice at ucusal value of the Bernot of the comparator 2555 initiately higher from that 6 from the Arror. The nominal action of the comparator is 0, as shown at 281 in Figure 11M. The comparator conse control algoral SENSE shown in Figure 11N is in 85 6 state, so the detaction sense of the comparator is 185 6 state, so the

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Sample storage

alightly exceeds the voltage of the

capachor 2545, the naminal output state of the comparator 255 and, hence, the state of the pass electrode

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pixel decizode remains in the 1 state during the first formation portion of the frame 1 Martination period, as a subministration period, as a subministration period, as a subministration period, as a subministration to the first properties of the first period of the

(D149) The raryo signal brocesses as the fame 1 its ministor period progresses. When the narry eignal signally crosests the voltage strend in the sample early expositive 244E, the norminal output of the companion of the output of t

moddator is Burnhestad (see Figuro 11C).
[0150] At the beginning of the frame 1 betance pariod, the level of the rame signal RAMP matums to sea, and the roaniel output of the comparatro 255 shown In Figure 11M danges from 1 to 0. The comparatro sense combo signal SENSE also changes from 0 to 1. so the state of the pixel electrode terrais unshanged (and opposite but that the moral parties of the frame 1 the through the first the profile of the first the through the first the profile of the beliance period, during the first therporal portion of the first the beliance period, so shown at 257 in Figure 1.

110.

(Pil61) The ramp signal increases as the trame 1 bell more period progresses. When the ramp signal significances the harm signal significances the voltage sized in the sample stange oppositor 250, the normal output of the comparator 255 shown in Figure 11M changes from 0 to 1. Since unchanged, the state of the pixel electrode strong changes from 0 to 1. Since the pixel electrode remains control signal remains changes from 0 to 1, as shown at 289 in Figure 11M. The pixel electrode remains in this state in the second lemporal portion conscituting the remainder of the farmal inhalmost period. The states of the drive merelocin in the first and socond temporal portions of the between the first and socond emporal portions of the between period are quivastic to those in the first and second temporal portions, respectively, of the first and second temporal portions, respectively, of the first and second temporal post is controct.

described. During the frame 2 illumination period, the Operation of the analog drive grout 214 quring the frame 2 illumination and balance periods is the same as during the frame 0 illumination and balance respectively, and will therefore not be analog other chask applies a drive signal to the plost The analog semple was stored in the cample storage It can be seen from Figures 11K and 11L that electrode in response to the arrelog sample of frame 2. ing which the drive eignal applied to the electrode 212 is capacitors during the previous frame. The analog samthe first temporal portion of the illumination period, durin the 1 state, depends on the level of the analog cample stored in the respective one of the sample storage log samplo of frama 2 has a relatively high larel. The tracked of the illumination period constituted by the first capacitor 254E during the frame 2 sample load period. ole of frame 1 lucs relatively low level whereas the una-

temporal pordons during the frame 1 Burninefron period and the frame 2 Burninefan period, hespecifiely, in regentres to frame unalcy samples deponds on the lenels of the analog samples.

10154) Figure 12 shows an example of a circuit first may be used as the switched-serse comparator 255 in the analog dilive circuit 214 shown in Figure 108.

The standard charles shown in rights 10c.

[DIGS] The competitive 255 is composed of the conventional competition 311, the output of which is kell to care input of the cack spansar. It is a subsidiaried form the chark pensars to right 12c. The convention is the base 250. When the counted signal SCHEZ is in the 1 stade, the detection sense of the competitive 251 is the campetitive signal SCHEZ is in the 1 stade, the detection sense of the competitive 311. When the competitive signal SCHEZ is in the 1 stade, the conventional competitive 311. When the competitive signal SCHEZ is in the 1 stade, the detection sense of the competitive 311.

ical embodiment, the column busses are long and have substantial especiance and therefore deby the analog tor described above, the analog camples are distributed to the place by the column busses 131,-1314, in a pracsamples transmitted along them. Moreover, comparing Figures 6D and 6J-6M shows that the control signal on almost at the same fime as the last englog sample of each line of the video signal is placed on the column bus to be loaded into the analog dine chants of the pixels at the right-hand side of the pixel array. The problem is sumpling arout 182, i.e., the pixels in the upper right of the pixel array in the examples shown in Figures 4A and [0156] In the embodiments of the spatial light modulaeach of the row salect busies 133-133, is de-esserted 1314. This, together with the konomission dolay on the column busses causes less than the full analog sample especially severe in the pixels thist are remade from the aul shown in Figure 19. The embodiment shown in The embodiments shown in Figures 10A, 15A and 16 104. The problem can be overcome using the embodiment 304 of the cample dorbration and distribution cir-Figure 13 is a variation of the embodiment of the sample derkation and distribution circuit shown in Figure 4A and uses the analog drive circuit shown in Figure 48. can be similarly modified. 8 R 18 ş

[0457] In the sample derivation and distribution circuit han at the certer of the pixel anay to form two sets of row schoot busses 133Ly-135Lg and 153Ry-139Rg. The 304 shown in Figure 19, the row select busses are broidithand row select busses 1891,-1831, are connected to the row select inputs of the analog othe crouits of the end 2 in the exemple shown) and to the output of the left-hand row selector 1341. The right-hand row solect inputs of the analog drive circuits of the pixels in the right-hand half of the pixel array (columns 3 and 4 in the busses 193Ry-183Ry are connected to the row select Externole shown) and to the cupput of the right-hand row picels in the laft-hand half of the phost array (columns 134R. The left-hand and right-hand now selec one are identical to the row selector 134 described 3

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United Department of the cample derhadon and destribution citrata strown in Figure 13 will now be described with retorence to Figures 144-145. Figures 144-140 respectively show the control signed weekoming on the control lines 189,-1894, controlled in the control incurof the SH thouths 189,-1894, during the picture period of one time or the wideo signal. An analog sample is placed on the respective columnias 131-131, at each falling cdgo of these waveforms.

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fortist of penation of lath tent row calcutor 1941, is clearly a described above with neglector 194 described above with neglector to the figures 6.4.64t. As exhown in Figure 144. Be control eighal on the new select bus 1934, swildnes to its 1 state at the beginning of the first like of lihe vidoo signal, and remains in list 1 state until the sint line. However, during the second haif of the first like, no carryphy to performed by the sample-and-hold drubs 198, and 1982, whose outdusters commercial via the column busses 191, and 191, to the analog drive circuits controded to the new select bus 1931., Accordingly, for analog drive circuits in the first love of the pixel and yith ser controded to the new select bus 1934, have a firm expectation analog compared of the pixel ser controded to the one select bus 1934, have a firm expressing to belout cre-half of the first like period to receive their respective analog compais.

have a time corresponding to about one-half of the line point of breauth after sepacitive arraptes.

Dividio Dreauthorn of right-hand four selector 154R is smile to that of the row selector 154 described stove with reference to Figures 64-6M, but is delayed by one-half of the line point. As strom in Figure 14F, the control of signal on the now select bus 158F, is in its 0 chair and demays to fits 1 state half with the line 10 chair and uning the first half of the first line of the video agree, and demays to fits 1 state half-way brough he first line pends. The change in state halfors place prior to the samples carpies of the first line of the video signal onto a the chair functor 158, and 158, footing any analog camples of the first line of the video signal onto the country forms of the cruits in the first line of the prior innity the one-body dive circuits in the first line of the prior innity the controlled to the naulog samples of the first line of the video signal when these enabog samples are put on the se respective odurn busses.

respective obtains busses.

Inspective obtains busses.

In file for faritation of the first line of the video signal, and for the first line of the video signal, and for the first line of the video signal, as shown in Figure 14ft. During the first half of the second line, no sampling to performed by the sample-en-chool order 138, and 138, whose adapta are connected with the column busses 131, and 131, to the analog diversity the enalog diversity the enalog diversity of the first row of the post circuits outniced to the row select bus 13581, According the time first row of the post and that he connected to the row select bus 13581, there is time corresponding to shout one-heal of the line period to receive first respective analog samples.

(1962) The row setectors 1341, and 1341 operate in a manner strater to that described during the remaining these 2-A of the trame of the Video signed.

POTCS] In the example chorm, he raw select buses are the buses are business. He is is and chicals the few or eached busses may be broken asymmetrically with an appropriate drange to the delay of the delay module 185. For examples, the decapitings be configured to that the tight row selector 194P controls only the arrange drive charake because near the would have insufficient time to receive their analog samples it has would have insufficient time to receive their analog samples it has would have insufficient time to receive their analog samples it has would have insufficient time to receive their analog.

10164) In the examples shown in Figure 14E and 14E, coach output of each now selector is in its 1 state for one states at the beginning and mid-point, respectively, of and the mid-point of line 2, respectively. However, as long as these control signals namen in their 1 for longer tine period. However, this is not critical. The control etg. nals on the row select busses 133L, and 133R, are line 1. However, the row select countrol signate may switch to their 1 states may switch to their 1 states at a time fater then the beginning and mid-point, respecfively, of line 1. Moreover, these control signeds are shown as reverting to their 0 states at the end of line 1 line 2, respectively. The setting time of an arralog drive shown in Figures 14E and 14F as awitching to their 1 than the longest secting time of the analog other dirouts connected to from, they may revent to their 0 states some time before the end of tine 1 and the mid-point of drouth is the time required for an analog sample to transfar fully to the enabg drive drout from the cample-and-hold drouit to which the areag drive drout is con-9 8

ID 1618. An example of a color display device based on the embodiment shown in Figures 4A and 48 is shown in Figures 15A and 168 in which dements corresponding to those in Figures 4A and 48 are tubosated by the same reference numerals. In the embosinest shown in Figures 16A and 168, the earnple special stopminest shown in Figures 16A and 168, the sample special or 16AP, 16AC and 15AP, or earnple or component of the color video signal. The parallel earnple derivation and distribution cloud 40A broades three sampling circulis 132A; 132A and 132B, one for each old component of the color video signal. The sampling circulis seath take arradog samples from one ord component of the color video signal and distribute from any circulis each take arradog samples from one ord component of the color video signal and distribute from any arradog samples to the respective sample as bardog samples to the respective sample are stopping array 102. The column color component-specific column busses for each ochorum in the pixel array 112. The column of three color component-specific column busses for each ochorum in the pixel array 112. The column of the component-specific column busses for the component-specific column busses for the component-specific column busses for the color component-specific column busses for the common of the color component-specific column busses for the common of the color column in the pixel array 102. The column of the common column in the pixel array 102. The column of the common column in the pixel array 102. The column of the common column in the pixel array 102. The column of the common column in the pixel array 102. The column of the common column in the pixel array 102. The column color component-specific column busses for the column color component-specific column busses for the column color component-specific column busses for the column color common column column

Forth, 2029 of the earlog (MING) in the offen signal generator 2029 of the earlog drive drough 15% for earnpie output fransisters 16% 1650 and 1659 opentie in response to the cequentially-explaint select control eginals.

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;2 the drive signate, one of the LEDs 69-71 illuminates the spatial light modelstor with light of a different color consequence, the manufact the arms to the coor component form which the arms to search of the order of the principle was derived. Outing the beliance period of each of the foreign each of the price is restincted. In this embodiment, the display period for rideo signal, the othe signal generator generates three to sequentially considers 154R, 154G and 154B to the ramp capadion log samples. During the Illumination period of each of each odor has a duration of one-third of the picture connect the analog sample stored in the comple storage 160 and the invertor 168. For each thems of the cater dithe signats, one in response to each of the three anaperiod at one frame of the color video signal. respectively,

[0167] The drive signal generator 328 shown in Figure 198 may incorporate the offset correction drauby show

B ¥ (0183) The preferred embodiment of a color deplay device uses the parallel sample devicement and dishibution along Arown in Figure 154 but with the emalog generator 328 shown in Figure 15B and the input 255 of the drive signal generator 228 of the analog drive drive circuit 414 shown in Figure 15C. The sample effection section 826 of the analog drive chould to the samo as that of the enalog office circuit 314 shown in fame 158. The drive signal generator 428 of the enalog drive chault 414 incorporates the sample output transistore 166R, 158G and 156B of the other signal draut 214 shown in Figure 10B. The Input change over abautly, composed of the transistors 2560, 2570, 256E respectively to sequentially connect the enalog sample stored in the sample storage capacitons 154R, 154G and 154B to the input of the comperator via the hour change-over dirautity and entitahed-series comparation and 257E and the control signals ODD and EVEN, is common nade of the sample output transistors 156H, 1569 and 1568 on one hand and the hours A and B of disposed between the ramp signal bus 262 and the I'v comparation 255 on the other. The comple output ransistons operate in response to the sequentially-exppilod select control signate RSEL, GSEL and BSEL, cheroe over circulary.

The Input change-over circuity operates in the input change-over circuity and to invert the sense of the comparator between the Rumination period and the response to the control signals EVEN and ODD. These red. The control eignal SENSE changes the detection senter of the comparation to take account of the action of control eignets change state in antiphase between oddnumbered and even-numbered frames of the video sigperiod. The input comparator average out in consecutive frames, as balance period of each display diange-over circuitry causes any docarbed above.

crouit 504 for use in a color display device based on the embodiment shown in Figures 10A and 10B is shown in An example of a seriel-load earmple derivetion

as frames of the color-soquential vision signal. Depending on the capabilities of the graphics adapter that generates the color video signal, the RGB sequencer 211 embodiment shown in Figure 10A are indicated by the same reference numerals. In the ambodiment shown in Figure 16, the arradog other circuits of the pizals is blantical to the analog drive drouit 214 shown in Figure 10B, and will not be described further. In the sample derive converts the color video signal to a color-sequential video signal in which the three color components of each fustrie of the color video signal are concatonated tion and distribution circuit 504, the RGB sequencer 211 corresponding to **elements** may be simple or more complex. to in which

[017] If the graphics autorior is cauchio of generaling a color-expuential video signel, the RCB sequences may be omitted if the graphics autorior is a conventional graphics activator capable of a frame rate of greator than 180 Hz, the RGB sequencer can be a three-way curitch. The emitch sequentially selects the component of a first frame, the green component of the ecound itsme and the blue component of the third frame greater than about 100 Hz, for example, and preferably Rd, green and blue color components of consecutive frames of the color video signal as the frames of the color-ecquential victeo signal. The smitch selects the red of the octor video signal as the first frame, the second keme and the third frame, respectively, of the colorequantial video signal. The sequence then repeats, i.e., the smith selects the renponent of the fourth frame of the color video signal as the fourth frame of the color-sequential video signal. R B 8

DITZ If the graphics adaptor is not capable of a high frame rate, the RGB sequencer 211 samples each color rarily stored, and then are sequentially read out in color component order with a clock speed of three times the to the original campling rate can be used, and two of sequential bit stream is then subject to digital to analog component of each frame of the color video signal. The samples derived from each color component are tempooriginal sampling rate. Alternatively, a clock speed equal every three samples not read out. The resulting adorconversion to generate to the color-sequential video sig-

(0173) The sampling chout 152 takes analog samples 242 and feeds the enalog samples to the column busses, in a firm corresponding to the frame period of from the color-sequential video signal at the rate of the rate of the phot clock generated by the clock generator the color video signal, each pixel of the pixel array portding to the three odor components of the frame of frame of the color-sequential video signal has been loaded into one of the sample selection sections of the receives a sample derived from each of three consecutive frames of the color-sequential video signal comehe color video signal. After an analog sample of each analog office circuit of each pivel considering the poxel 202, the wavefarm generator of the analog drive À 9 8

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repording to the color companent from which the article surpule was derived. In the balance period of the display period, the drive signal restores the DC balance kg semple. During the Illumination ported of the display period of the drive signal, one of the LEDs 69-71 library. neties the spatial light modulator with light of a color conof the pixel. In this embodiment, the display period has draft generates a drive signal in response to the araa duration equel to the frame period of the colorsoquential video signal.

doorbed with various exemplary logic states, signal states, transistar types and rows and columns, the Although the above embadiments have been embaciments can have apposite logio states, aignal Although this disclosure describes Australive embodiments described, and their various modifications stood that the invention is not limited to the precise embodiments of the Invention in detail it is to be underclates, bansistor types and rows and columns. [9174] 0175

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R An emadog drive circuit (114, 214, 314) for othering a picel electrodo (118) in response to an analog sample demed from a video signal, the analog office circuit comparising:

8 a sample caledron section (128, 2250, 229E, 825) that receives and temporarily stores the origing sample during a sample load period;

₽ Ð Bequence of a first temporal portion and a sec-ord temporal portion, the tirst temporal portion e drive signal generator (128, 228, 328, 428) trade, the drive signal being compassed of a that, during a display period that tollows the sample load poriod, gonerates a drive signal and explies the other signal to the pixel cleahaving a time duration substantially propor-In the earnple selection section, the second temporal portion being a temporal complement borral to the auxilog comple temporarily stored of the first temporal portion.

# The arratog artive circuit of claim 1, in which: d

8 analog sample only when the analog sample is taken from one of the odd frames; the victeo signal is compassed of efferneting oct the surple selection section is an odd sample selection (2260) and receives and stores the and even frames each having a frame period;

no analog drive circuit additionally comprises en even sample selection section (226E) that receives and stares the analog sample when he analog sample is taken from one of the

frames; and

is taken from one of the even frames, the chive signal generator generates (228) the drive signal nal in response to the enaby earning scred in the add sample selection section, and, during a display period coincident with each earning load period in which the analog sample is taken during a display period exincident with each generator generates the drive signal in response to the analog sample temporarily load period in which the analog sample from one of the cool frames, the drive signal stared in the even cample selection conform The analog drive circuit of dainn 1 or 2, in unlich the video signal la a color-sequential video signal.

The anelog othre circuit of claim 1, 2 or 3, in which The drive signed generator operates in response to a remp signed that has a non-finear slope to provide gemma correction

hay be practiced within the scope of the invention

seaned by the appended claims.

The analog drive drout of any one of claims 1-4, th which the sample storage section (126, 2260, 2265, 326) includes: ಸ

a cample storage element (154, 2540, 254E,

ISAR, 1540, 154B);

of elond period to activit the analog sample to 158G, 156B) that opens one of (a) during and (b) prior to the display period, the sample out-put gate being disposed between the sample stonege of ement and the drive signal generator a sample selection gate (152, 2520, 252E, 152R, 152B, 152B) that opens during the sem-The sample storage element and that is closed a cample output gate (158, 2560, 256E, 156R, during the display period; and 128, 228, 828)

The analog drive circuit of any one of claims 1-5, in į

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the drive signal generator (228) includes a comparator (255) that generates the othe sigral, the comparator comprising a first input (A) to which a ramp signal is connected, the ramp signal having a dumbion equal to the deplay period, and a second houd (B) to which the sample selection section is connected; and when the analog dive circuit includes add and the analogichte circuit additionally comprises a smitching element interposed between the owen sample selection socions (2260, 2265), sample calection sections and the second imput

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the ood sample selection section and the even sample relation section to the second input of of the comparator, and alternately commoding the comparator in consecutive display periods.

(228) Includes a

signel generator

nal end has a detection sense set by a sense control signal (SENSE) that changes state half-way fivough the display period, the comparator comparator (225) that generales the drive sig-

7. The smallog of the circuit of any onto of claims 1-6, in

the drive signal generator (128) includes:

an invortor (166) that generates the drive signal, the inverter having an input and an (159) and a second cleatrade (161), the expecialor (160) Iraving a first electrode lirst electrode boing connected to the input of the inverter and to the sample colection

8 when the analog drive draft includes odd and he analog drive circuit additionally comprises a tion section and the even sample refection sec-tion to the first electrode of the capeation and between (a) the sample solection sections and (b) the first electrodo of the capacitor and the alternately connecting the odd sample saleooven sample selection sections (2260, 226E), ewildning chament (2580, 250E) Interposed the input of the inverter in consecutive display input of the inverter, the subbling element

8. The analog office circuit of any one of claims 1-5, in

\$ 6 he second temporal portion is a linst sequence erates the drive signal in a first electrical state BALANCE) of the first temporal portion, in the sequence of the first temporal portion and (a.g., ILLUM) of the first temporal portion and the second formoral portion and has a duration the drive signal generator (129, 228, 328) genduring the first temporal portion and in a socwhich the drive aignal is in the second electrical and the second temporal portion, in portion, and generates the drive signal eddifonally composed of a second sequence (e.g., state, the Pret temporal portion and the second tamporal portion being in any order in the eacand electrical state during the second tempons which the other eignal is in the first electrical oqual to one half of the display period; and

a first input (A) to which a ramp signal har-ing a chratian equal to one-half of the dis-play period is cornected, and

second input (B) to which the sample when the enaby office circuit comprises odd and even asmple selection accions (2200, 226E), the analog drive circuit additionally a switching element interposed between the sample selection sections and the second input of the comparator, the switching dement alternately connecting the cold sample selection section and the even cample selecdon section to the second input of the comparaselection section (128) is connected, and for in consecutive display periods.

8

a reset swatch (164) that discharges the

being connected to a ramp signal, and

attector prior to the display period; and

section (126, 826), the second electrode

The analog office circuit of claim 1-5 or 8, in which: 렫

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the drive signal generator (228) includes a comparator (255) that generates the dive signal, the compountor comprishing a first input (A) and a second input (B) and having a delection sensa sel by a same control algual (SENSE) having opposite states in consecutive display periods; and the aralog drive circuit additionally includes:

elternately connects a ramp signal to (a) the first input and (b) the second input of a first switching element (2570, 257E) that perfods, the ramp signal having a dustion when the analog date draut comprises a nacts the sample selection saction to (a) the second input and (b) the first input of play periods, and, when the analog drive selection sections (2260, 2285), a second switching element (2560, 2565) that alterthe comparator during consecutive display switching element that effernately conthe comparator during the compactive dedrout comprises odd eard even sample nately connects (a) the odd cample selecsection to the second imput of the postator and (b) the even sample selensingle sample selection section, a second ecction to the first input of the compaof one half of the display period, and Ē

11. The analog office circuit of claim 8, in which the

rator during the consecutive frame periods.

The arreing othe circuit of claim 8, in which:

œ

and sequence.

Z

sample output gale (158R, 196G, 156B)

Ç

Yive signal generator (128) includos:

a first inventer (166), the first inventer having an

second inverter (174) having an input conrected to the output of the first inventer, the Second inverter having an output.

trode being connected to the input of the first a capadior (160) having a tinal electrode (169) and a second electrode (1811), the first elechwerter and to the sample selection saction, the cocond electrode being connected to a ramp signal having a duration equal to one-half

a rocat switch (164) that discharges the capacof the display perfect:

ord inverse and operating in response to a seree control (SENSE) that changes as table half-way frough the display period to take the cutput of one of (a) the first invertor and (b) the second invarier as the drive light a smitching arangement (176, 178) connected to the outputs of the first inventor and the secfor prior to the display period; and

12. The amalog drive circuit of claim 7 or 11, in which;

the drive signal generator additionally includes:

roud of the inverter to the sumple edection se coupling capacitor (201) coupling the

comparator in conscioutive display periods. an additional switch (200) that temporarily.

connects the output of the first inverter to

section, and

the input of the first inverter prior to the dis-

play period; and

15. The enalog drive cloud of claim 1, in which:

poral portion each have a beginning; and the drive signal is composed of pulse having a raf portion and a pulse having a second polar-ity, opposite the first polarity, of the baginaring of the second temporal portion. the first temporal portion and fre second temfirst potarity at the beginning of the first tempo-

\$

predictermined invester freshold voltage when for additional switch connects the cutour of the first inverter to the troot of the first inverter.

agnet (SCLEAN) that has a state equal to a

the reset switch (184) is coupled to a reference

d'Ne signal generator includes an a.c.-coupled out-16. The analog office circuit of claim 16, in which the

sample output gates operating sequentially to connect the arralog cample stored in each samlocated between each eample storage element and the drive signal generator (328, 428), the pie storage element to the drive signal genera 2

tiofly generates a drive signal in response to the drive signal generator (328, 428) sequenthe analog sample stored in each sample storage element.

The arealog drive chout of claim 13, in which:

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the drive signal generator (428) includes a nal, the compension comprising a first input (A) and having a delection having opposite states in consecutive framo periods; and comparator (2.55) that generales the drive eig sense set by a sense control signal (SENSE)

he arelog drive drait additionally comprises:

a first switching element (2570, 257E) thai alternately corryades a mmp signal to (a) the first input and (b) the second input of ods, the ramp signed having a duration of the comparator in consecutive frame peri-

a second switching element (2560, 258E) put gates to (a) the second input of the comparator and (b) the first input of the that attentiately connects the sample outone-half of the frame period, and

18. The anelog dive circuit of claim 1, in which:

the video signal includes a color component for the sample selection section (329) includes: each of more than one colors; and

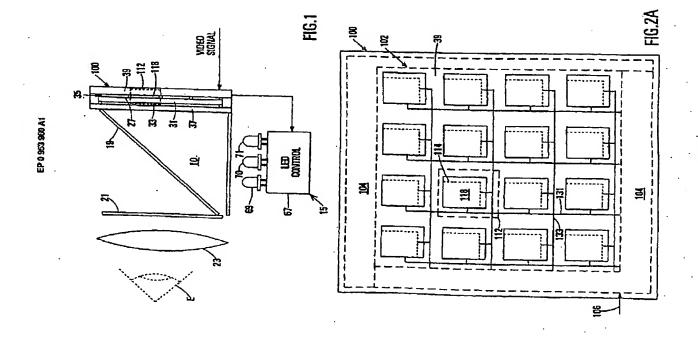
a sample clongs element (154R, 154Q, 154B) corresponding to each order compoa cample selection gate (152R, 152Q, nert, and

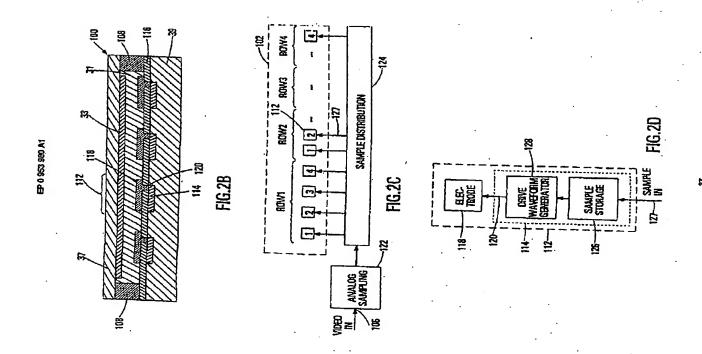
the analog other circuit edditionally compulses a

color component to each respective sam-1528) that opens during the sample load period to admit the analog sample of each

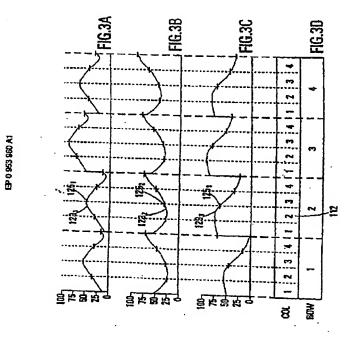
ple storage element, and

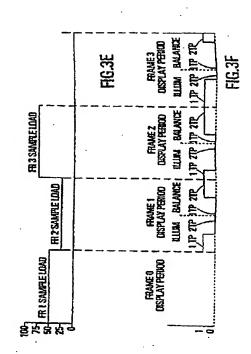
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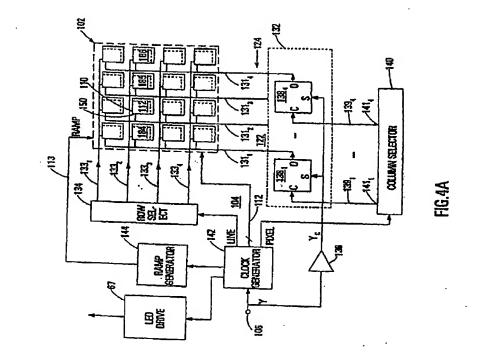
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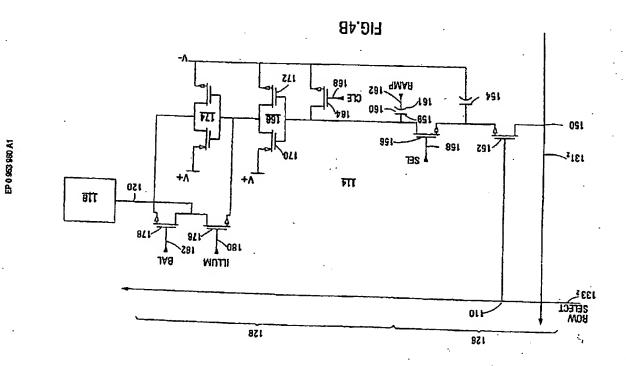


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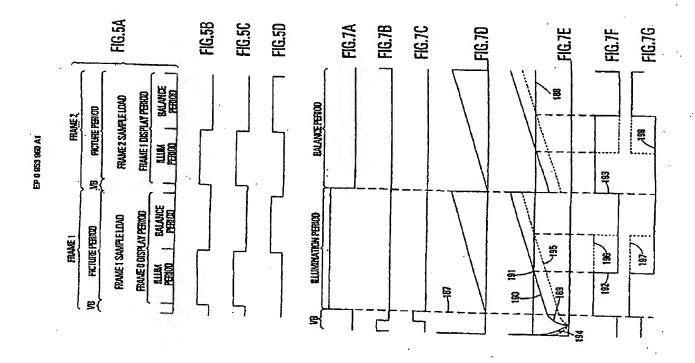
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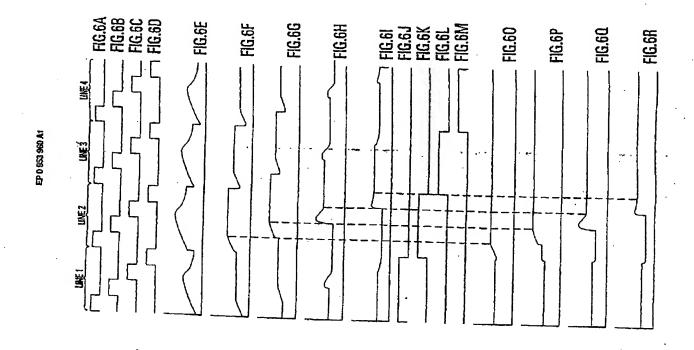


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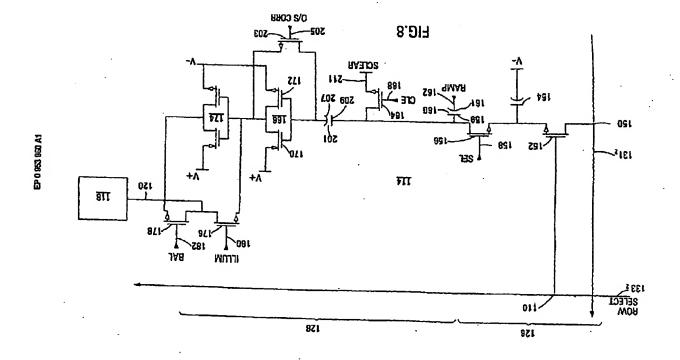


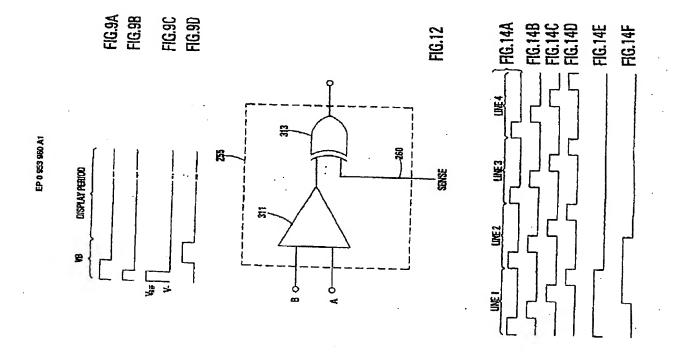
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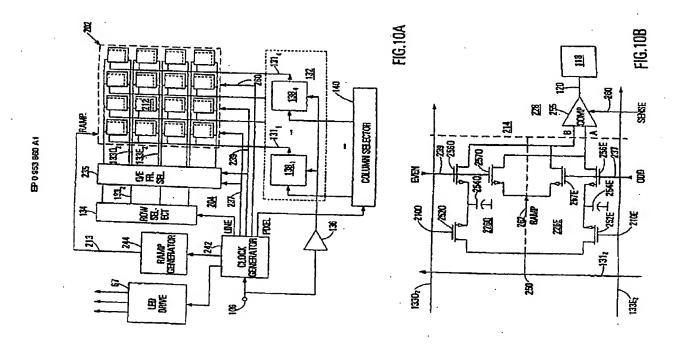


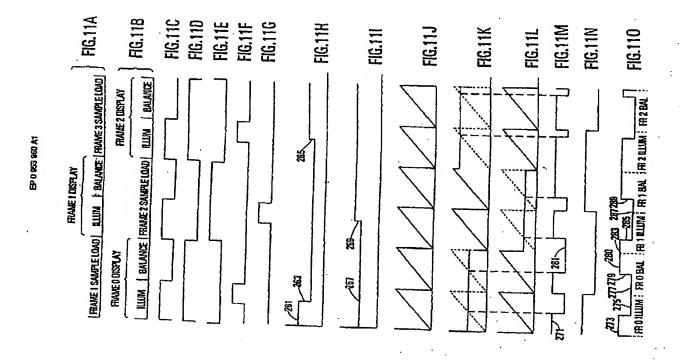


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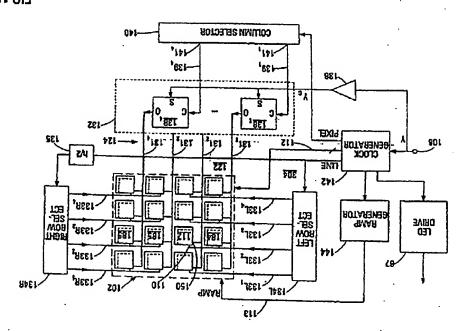
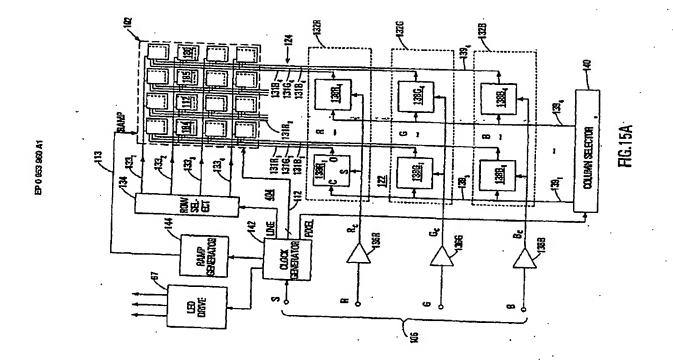
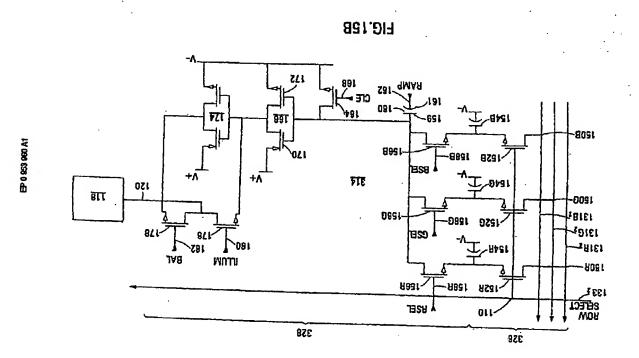
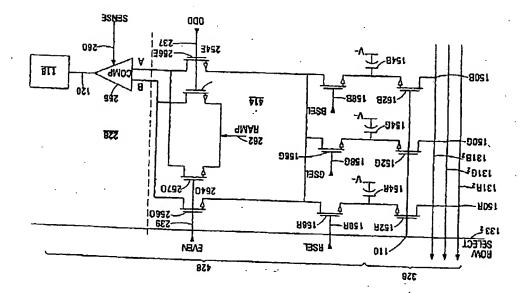


FIG.13

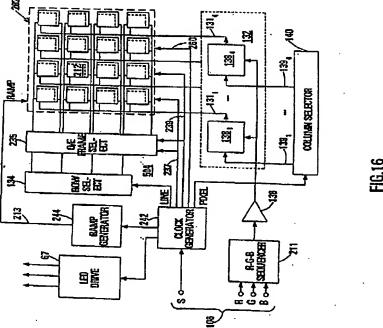




### FIG.15C



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